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TOPICAL REVIEW

Review of the 800-VDC Power Delivery Architecture and Isolated 800-V to 48-V Converter Solutions for Future AI Data Centers

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ABSTRACT The rapid growth of artificial intelligence (AI) workloads is increasing rack power demand in AI data centers. This trend is exposing the limitations of the conventional 48 VDC rack distribution and has motivated growing interest in higher-voltage power delivery architectures. This paper reviews the emerging 800 VDC power delivery architecture for future AI data centers and the isolated DC–DC converter solutions for the key 800 VDC to 48 VDC conversion stage. First, the motivation for adopting 800 VDC, the overall architecture, transition pathways from existing systems to 800 VDC deployment, and key facility-level components are discussed. Then, the main converter candidates for the 800 VDC to 48 VDC conversion stage are examined, including the half-bridge LLC resonant family, the full-bridge LLC resonant converter, the three-level half-bridge LLC resonant converter, and the three-phase LLC resonant family. The literature reviewed in this article indicates that 800 VDC can reduce current and cabling burden and can support higher rack power density, while 800-V converter selection involves tradeoffs among switch voltage stress, power handling capability, magnetic complexity, modularity, and implementation maturity. This paper also shows that achieving high efficiency and high power density in the 800 VDC to 48 VDC stage remains closely tied to challenges such as high secondary-side current, magnetic integration, control and modulation limitations, and thermal management.

INDEX TERMS Artificial intelligence (AI) data center, 800 VDC architecture, DC–DC converter, power supply unit (PSU), LLC resonant converter, DC transformer (DCX).

I. INTRODUCTION

Artificial intelligence has been widely regarded as one of the most influential technologies of the 21st century, and major impacts on society and the economy are anticipated [1], [2]. The global AI data center market is projected to grow at a compound annual growth rate (CAGR) of 28.3% from 2025 to 2030, with North America holding the largest market share [3]. In the United States, investment in energy-intensive data centers has increased in anticipation of future AI demand and AI monetization [1]. In recent years, Information and Communication Technology (ICT) investment as a share of gross domestic product (GDP) has reached its highest level in three decades, rising to around 5.5% of U.S. GDP and being driven mainly by investment in corporate software, networks, and data centers [1]. The modern wave of AI, particularly generative AI, has been enabled by advances in hardware and breakthroughs in model architectures and algorithms, and has led to the rapid growth of AI workloads [2].

The growth in AI workloads has significantly increased data center power demand and has propelled the emergence of hyperscale facilities [4]. A hyperscale AI data center is described as having a capacity of 100 MW or more and consuming as much electricity annually as about 100,000 households [1]. In 2024, electricity consumption from data centers in the United States was estimated at around 180 TWh, accounting for 4.4% of total U.S. electricity consumption [1]. Nearly half of U.S. electricity demand growth to 2030 has been projected to result from data center growth [1]. With the increased power demand and operational limitations of

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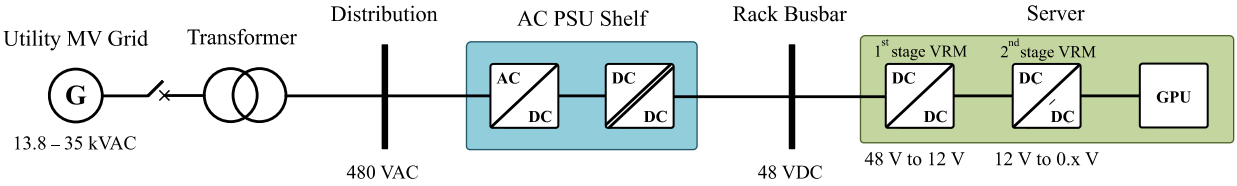


FIGURE 1. Current power delivery architecture with 48 VDC rack busbar distribution for AI data centers.

the current AI data center power delivery architecture, this architecture is expected to be redesigned for higher-power operation [4], [5].

The current AI data center power delivery architecture with 400/415/480 VAC rack-level distribution and 48/50/54 VDC rack busbar is illustrated in Fig. 1 [6], [7]. In this architecture, which has facility-level and rack-level AC distribution and in-rack DC distribution, power supply units (PSUs) and voltage regulator modules (VRMs) are used to feed the graphics processing units (GPUs) [7], [8]. Power is delivered to each rack at 400/415/480 VAC, where an in-rack PSU is used to convert the input to an intermediate bus voltage (IBV), typically in the 48/50/54 VDC range [6], [7], [9], [10]. The PSU is a device that converts AC or DC input power to one or more DC power outputs [3]. Inside the PSU, a two-stage conversion is commonly used, in which the first stage incorporates power factor correction (PFC) operation and generates an approximately 400 VDC bus, and the second stage is an isolated DC–DC stage that converts this bus to an IBV for the motherboard supply [8]. Standardization of PSU requirements has been provided by the Open Compute Project (OCP), which is an industry collaboration for open and scalable data center hardware. Relevant OCP specifications for 48 VDC data center power delivery architecture, including onboard power solutions, power shelves, and rack PSUs, are documented in [11], [12], and [13]. The OCP Open Rack V3 PSU specification has set efficiency targets of >97.5% peak and >96.5% minimum over the 30%–100% load range [13].

Today's IT racks typically operate at power levels in the 10–30 kW class [6]. Emerging rack-scale AI systems such as NVIDIA GB200 NVL72 and NVIDIA GB300 NVL72 are pushing rack power into the 120-kW class, and NVIDIA's roadmap toward Kyber racks powered by Rubin Ultra GPUs is targeting >1 MW-class racks [14], [15]. In the current 48 VDC rack busbar distribution architecture, as rack power density increases, the current supplied to the racks also increases, which necessitates a larger number of parallel power cables [14]. To address this challenge, the distribution voltage should be increased, allowing both the number and thickness of power cables to be reduced [14]. As a result, heat generation can be alleviated and material cost can be reduced by lowering cable losses and copper usage [16], [17]. In [16] and [17], a 100 kW data center in Japan was evaluated under two rack-level voltage distribution systems, 400 VDC and 48 VDC. Under the same allowable cable current and voltage-drop constraints, the required copper volume for cabling was reported to be nearly fifteen times lower in the 400 VDC distribution than in the 48 VDC distribution.

Meeting these unprecedented rack-level power requirements has driven growing interest in higher-voltage solutions, and the 800 VDC architecture was introduced by NVIDIA in 2025 for next-generation power distribution in AI data centers [6], [14]. The 800 VDC power delivery architecture is proposed to accommodate both near-term 120 kW-class racks and future 1 MW-class racks [14]. Furthermore, it is capable of improving end-to-end efficiency by up to approximately 5% compared with today's 48 VDC systems [14]. In addition, compared with the 48 VDC in-rack distribution system, the 800 VDC in-rack distribution system is reported to reduce current levels and cable bulk while remaining scalable and compatible with modern data center safety practices [4], [6]. Therefore, the transition toward the 800 VDC architecture is essential for future AI data centers, and power electronic technologies for suitable 800 VDC-to-IBV conversion are critical.

In this paper, the 800 VDC power delivery architecture for future AI data centers is discussed. In addition, potential power electronic solutions for the key 800 VDC to 48 VDC isolated DC–DC conversion stage are reviewed. The organization of this paper is as follows. In Section II, the 800 VDC power delivery architecture is discussed. In Section III, the governing equations and design principles of LLC resonant converters operating in DCX mode are presented. Section IV then addresses the magnetic design of these converters. Sections V through VIII review the four primary converter families: the half-bridge (Section V), the full-bridge (Section VI), the three-level half-bridge (Section VII), and the three-phase (Section VIII) LLC resonant converters for 800 VDC to 48 VDC conversion. Finally, in Section IX, a comparison of these topologies is provided.

II. 800 VDC POWER DELIVERY ARCHITECTURE

The rapid growth of generative AI is turning conventional data centers into "AI factories", where power delivery is becoming a primary constraint on system scaling and deployment [18], [19], [20]. As GPU clusters become denser, rack power is increasing, which places growing stress on existing power delivery approaches [10]. A clear example is the leap from the NVIDIA Hopper architecture (2022) to the NVIDIA Blackwell architecture (2024), with rack power rising from about 40 kW to about 120 kW [14], [15]. In this transition, performance for a single user is associated with roughly

TABLE 1. Power transfer capability for different distribution voltages under identical current constraints.

Voltage	Wires	Power per cable diameter (kW/mm^2)	Power increase referred to 415 VAC
415 VAC	4 (P1, P2, P3, PE)	0.6	-
480 VAC	4 (P1, P2, P3, PE)	0.8	+ 16%
800 VDC	3 (POS, RTN, PE)	1.7	+ 157%
1,500 VDC	3 (POS, RTN, PE)	3.1	+ 382%

50 times higher tokens per second (TPS), while the thermal design power (TDP) of an individual GPU increased by about 75% and rack power density increased by about 3 times [10]. With Kyber racks moving toward the 1 MW-class range, traditional 48 VDC in-rack distribution becomes physically and economically impractical, and the 800 VDC architecture is proposed to scale power delivery more efficiently for next-generation AI rack densities [14], [15].

A. MOTIVATION TO 800 VDC ARCHITECTURE

Although traditional 48 VDC architectures have long enabled data center power scaling, several practical constraints emerge when supporting rack power beyond the 120-kW class, as highlighted below:

- *Excessive power loss and current limit*: At the rack level, low-voltage 48 VDC distribution requires very high current to deliver increasing power, which leads to severe resistive losses and increased heat generation [21]. In addition, AC whip ampacity is limited, since typical whips are rated at 60 A or 100 A, and allowable current is constrained by thermal limits and connector standards such as IEC 60309 [6], [22].
- *Physical integration and scalability constraints*: Higher rack power often requires more and/or larger rack power inlets, which consumes rack space and complicates cable management [6]. Managing and protecting multiple AC feeds adds design complexity and increases the equipment footprint [6], [23]. In addition, thick, heavy copper cabling consumes rack space, restricts airflow, and increases material and infrastructure costs, which limits practical scaling to higher rack power [4], [21], [24].

The benefit of higher distribution voltage can be shown by considering how much power can be carried through a fixed conductor size. For a fixed wire gauge with a 48 A continuous rating, Table 1 indicates that increasing the rack-level distribution from 415 VAC to 800 VDC allows approximately 157% more power to be transmitted through the same copper cross-sectional area under identical current constraints [6]. In North America, a common approach for increasing delivered power using existing infrastructure is to move from 415 VAC to 480 VAC, but this change provides only about a 16% increase under the same conductor and current constraints. Looking further ahead, 1500 VDC rack-level distribution is shown to enable an approximately 382% increase in transferable power through the same conductor sizes.

800 VDC rack-level distribution has been proposed to address these challenges and provide several advantages, as highlighted below:

- *Fewer conversion stages and improved efficiency*: The overall 800 VDC architecture can be streamlined by migrating AC–DC conversion upstream from the rack to the facility level and, ultimately, toward direct medium-voltage AC–DC conversion [6]. By converting grid power directly to 800 VDC at the data center entrance, intermediate conversion stages can be eliminated, and overall efficiency can be increased by up to 5% [14]. By removing unnecessary stages, a leaner and more efficient structure is achieved, with fewer equipment layers, reduced cost and space, improved reliability, and faster deployment [5], [10].
- *Reduced copper usage*: By increasing distribution voltage, lower current is required for the same power, enabling thinner cables and reducing copper usage by up to 45%, while also lowering cable weight and volume and improving cooling efficiency [14], [21].
- *Simpler rack interface*: The power interface to IT can be simplified, since an 800 VDC approach can enable a more streamlined physical interface to the rack and can markedly reduce the number of cables and components [4], [10].
- *Support for extreme rack power density*: Direct compatibility with high-power GPU racks is supported, because a higher rack busbar voltage can reduce conversion and routing volume in the compute space [10]. The 800 VDC system has been described as being designed to safely and efficiently support extreme AI rack power levels, including cases that can exceed 1 MW per rack [21].

Several practical challenges must also be addressed for 800 VDC architecture deployment. The higher voltage demands robust insulation, advanced protection, and specialized components that can operate safely within the confined space of standard server racks [2]. In addition, thermal management becomes more critical because compact, higher-power supplies dissipate more heat, and electromagnetic interference as well as isolation and grounding design must be carefully managed to ensure stable and safe operation in dense AI-focused environments [25], [26].

The viability of high-voltage DC distribution has also been demonstrated in adjacent industries, and these examples can serve as reference points for AI factory power systems. In electric vehicles, platform voltages have progressed from 400 VDC toward 800 VDC and above [27], [28], [29], [30], [31]. In photovoltaics, utility-scale PV installations commonly operate with DC buses in the 1000–1500 VDC range [32], [33], [34], [35], [36], [37]. These sectors indicate that mature equipment options, safety strategies, and operational

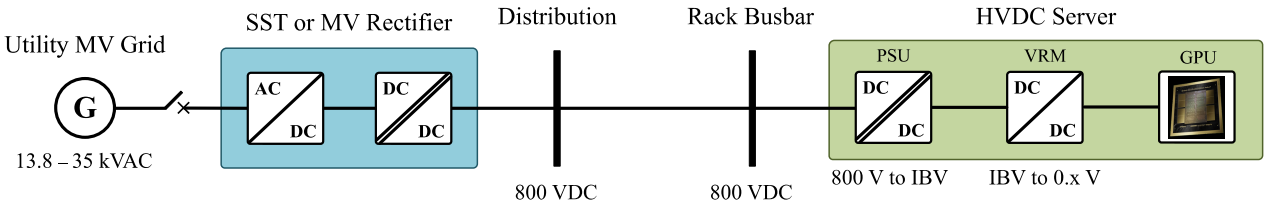


FIGURE 2. 800 VDC power delivery architecture for next-generation AI data centers.

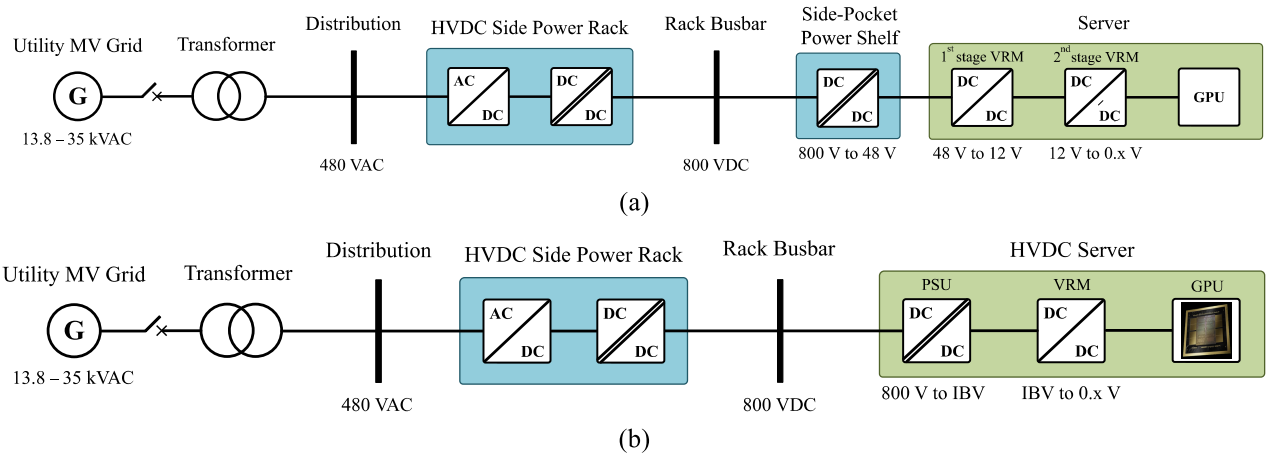


FIGURE 3. Transitional 800 VDC power delivery architectures based on side power rack: (a) 48 VDC server, (b) 800 VDC server.

practices already exist and can be adapted to the needs of AI Factory deployments.

B. THE 800 VDC ARCHITECTURE SCHEMATIC

The 800 VDC architecture schematic is illustrated in Fig. 2 [6], [38]. In this schematic, a medium-voltage (MV) rectifier or a solid-state transformer (SST) is used as the front-end interface for converting MVAC to the 800 VDC bus. These MV rectifier and SST are intended to enable direct conversion from MV levels (e.g., 35 kVAC) to 800 VDC, which can remove the need for the conventional low-voltage distribution layer (e.g., 480 VAC) and simplify facility-level power delivery. The size of MV rectifier and SST units has been reported to reach approximately 7.5 MVA per unit, with efficiency of 98.5% or higher [6].

This architecture aims to bring 800 VDC directly into the rack and distribute it to the compute node [10]. Inside the rack, the PSU first converts 800 VDC to an intermediate bus voltage, which is 48 VDC in early generations. The onboard VRMs then step this IBV down to the 0.x V (less than 1 V) rails required by the GPU domains. In this architecture, the DC–DC conversion stages are pushed as close as possible to the GPU to take advantage of the 800 VDC bus, minimizing power overhead in the system and reducing copper volume [39]. [40] states that, for future AI data center designs, it is desired to reduce the intermediate bus voltage to levels below 48 VDC, to 12.5 VDC or even 6.25 VDC, to improve efficiency, simplify point-of-load regulation, and reduce power-delivery complexity. For a design in which the intermediate bus voltage is assumed to be 12.5 VDC, direct conversion from 800 VDC to 12.5 VDC is performed, and the 12.5 V rail is routed only a short distance to the VRMs. This direct step-down can be implemented using a 64:1 converter, eliminating the separate 800 VDC to 48 VDC and 48 VDC to 12.5 VDC stages. Compared with a multistage approach, this direct conversion has been reported to provide approximately 1% additional efficiency improvement and about 26% area reduction, which is particularly valuable near the GPU where space is most constrained [6].

C. TRANSITION PATHWAYS TO 800 VDC DEPLOYMENT

Two transitional architectures can be established to transition from the existing 48 VDC architecture to the 800 VDC architecture by interfacing with existing facilities and relocating some conversion stages outside the IT rack. The first transitional architecture is illustrated in Fig. 3(a) [6], [38]. In this architecture, rack-level distribution remains at 480 VAC, and a two-stage AC–DC conversion is used to generate 800 VDC for in-rack distribution. The side-pocket power shelf is added in the IT rack to convert the 800 VDC rack busbar voltage to 48 VDC, which is then stepped down to 12 VDC by the VRMs before being regulated to the 0.x V rails required by the GPU. This approach is mainly motivated by near-term deployment needs, since full 800 VDC facility equipment and operational readiness may not yet be broadly available. Although the additional conversion stages make this solution

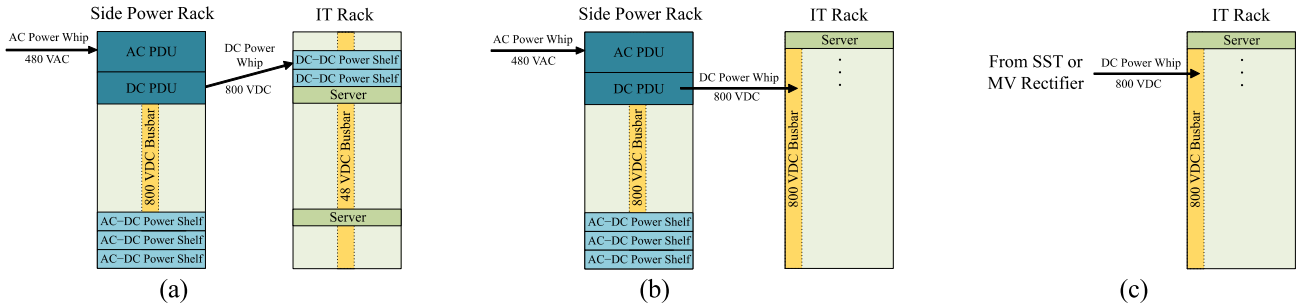


FIGURE 4. Rack configurations for different 800 VDC power delivery architectures: (a) side power rack alongside an IT rack with 48 VDC servers, (b) side power rack alongside an IT rack with 800 VDC servers, and (c) direct 800 VDC delivery to the IT rack with 800 VDC servers.

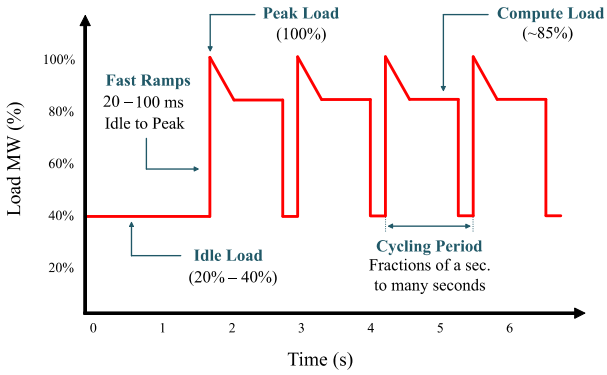


FIGURE 5. Example of rapidly varying power demand in AI data centers.

non-optimal from an end-to-end perspective, it enables higher IT rack densities by shifting power conversion hardware out of the IT rack and into a separate rack-scale power block.

The dedicated "side power rack" houses rectifiers and power distribution units that perform local AC–DC conversion for each rack [41]. The side power rack, placed adjacent to the IT rack, can be added in retrofit scenarios to preserve white space, the dedicated raised-floor area designed to house, power, and cool critical IT equipment, while minimizing disruption to the IT area [41]. As 800 VDC distribution hardware and data center operational practices mature, the side power rack can be phased out and replaced by higher power-density rectification located further upstream in the power distribution chain [6], [41].

The second transitional architecture is shown in Fig. 3(b) [6], [38]. In this architecture, the 480 VAC rack-level distribution voltage is converted to 800 VDC in the side power rack. The IT rack is equipped with an HVDC server that is fed directly from the 800 VDC rack busbar. Inside the HVDC server, the PSU converts 800 VDC to the intermediate bus voltage, and the VRM stage regulates the IBV to the 0.x V rails required by the GPU. Overall, this approach, compared with the first transitional architecture, can simplify power delivery and provide scalable support for high-density compute. Consistent with the goal of reducing conversion stages in the transitional architectures, [7] shows that data center power-delivery architectures with fewer power-conversion stages generally achieve higher overall end-to-end efficiency and higher reliability. The rack configurations for transitional and final 800 VDC deployment are summarized in Fig. 4 [6], [38], where the side power rack is shown to be used in the transitional architectures and to be removed in the final 800 VDC architecture [41], [42].

D. KEY FACILITY COMPONENTS OF THE 800 VDC ARCHITECTURE

Facility-level 800 VDC equipment for AI factories must be designed to maintain grid stability and power quality while supporting rapid load growth [6]. Large-scale AI training with thousands of GPUs can introduce substantial variability in power consumption, with frequent swings between high- and low-usage phases, as illustrated in Fig. 5 [2]. Reported workload profiles indicate short-cycle power variations on the order of about 50% of peak load, with transitions from an idle level of approximately 20%–40% to sharp peaks approaching 100% [2]. While 800 VDC implementation can improve efficiency and scalability at high power, it does not directly resolve this workload volatility [10]. Without appropriate smoothing and filtering, such rapid ramps and idle-to-peak transitions can create transient demands that degrade power quality and can even drive damaging power-system oscillations, potentially imposing significant torsional stress on turbine–generator drivetrains [2]. Therefore, energy storage is treated as an essential, active part of the architecture, and stabilizing AI power usage requires storage to be distributed across the data center infrastructure to buffer fast GPU power swings from utility-grid stability constraints. Because these fluctuations span multiple timescales, a multi-layer storage approach is typically deployed at both the in-rack level and the facility level within the power architecture [10].

At the in-rack level, short-duration storage, in the millisecond-to-second range, is implemented using high-power capacitors and supercapacitors placed close to the load [10], [41]. These in-rack devices are often referred to as capacitor bank units (CBUs). They absorb high-frequency power spikes and fill brief power valleys associated with AI workload dynamics, and response times as fast as 400 μs have been reported [6], [9], [10]. In addition, battery backup

units (BBUs) are also used in modern data centers, providing localized backup power within the rack. Compared with traditional AC UPS systems, BBUs equipped with lithium-ion batteries offer several advantages, including a longer lifespan of up to 10 years, a compact design that occupies 50–70% less space, and faster charging speeds [3]. BBUs are designed to support in-rack level power and can maintain the load for about 5–15 minutes [3]. At the utility-interconnection and on-site generation interface, a facility-level battery energy storage system (BESS) can be deployed to manage steadier, slower power variations. In the seconds-to-minutes range, BESS can mitigate larger workload ramps and provide ride-through capability during transfers to backup generators [6], [43]. Furthermore, it also supports load averaging and grid-forming functions to maintain a stable 800 VDC supply to sensitive compute infrastructure [43].

Within the front-end conversion chain, an SST-based system can be viewed as an integrated platform that combines a medium-voltage AC intake, power rectification modules, and a DC output distribution section [6]. Such a compact, high-capacity implementation is intended to support increasing rack density and to reduce the floor-space burden of DC power equipment. Recently, SSTs have attracted growing interest in different applications [44], [45], [46], [47], [48], [49], [50], [51]. In an SST, energy is processed by semiconductor devices at high frequency rather than by a transformer at line frequency, which can increase the power density of the power-supply system [44], [45]. As an example for data center applications, full-load efficiency of 98.1% has been reported for a 25 kW laboratory prototype converting 3.8 kVAC to 400 VDC using 10 kV SiC devices [50], [51]. However, extending SST capacity to multi-megawatt levels remains challenging due to rectification-module reliability and high-density electrical stresses, while protection, robustness, complexity, and scalability to arbitrary MV levels remain major concerns [52].

As an alternative to the evolving SST approach, medium-voltage rectifiers represent a mature option to be a high-power DC source [6]. MV rectifier systems have been widely used in applications such as mining [53], electrolysis [54], [55], rail [56], and grid-scale energy storage systems [57]. A typical implementation includes a step-down transformer, rectification modules, filtering stages, and protection subsystems. Because of their established design, MV rectifiers offer high reliability and strong supply-chain readiness. For near-term 800 VDC deployment, MV rectifiers can therefore provide a faster and more proven path than SST-based solutions [6].

Facility-level power equipment must prioritize both resilience and scalability. Resilience depends on robust protection, effective fault isolation, and redundancy across power paths to sustain operation during faults or maintenance [9]. Scalability requires a modular design that enables capacity expansion without major rework while maintaining safety and efficiency [9]. Key development needs include high-capacity rectification, advanced DC distribution boards, coordinated DC protection devices, clearly defined isolation points for safe service, simplified rack power interfaces, and integrated DC energy storage to manage dynamic power swings.

E. OTHER HVDC BUS DISTRIBUTION OPTIONS

Besides the 800 VDC bus, two other rack-level DC distribution approaches have been considered for data centers. The most prominent is the bipolar ±400 VDC bus, introduced by OCP in [9], which is technically feasible and can be viewed as a variant of the 800 VDC architecture. Its defining feature, the grounded midpoint, creates a three-wire system with +400 V, 0 V, and −400 V rails. The lower pole-to-ground voltage compared to the 800 VDC bus relaxes the clearance and creepage distances required by insulation-coordination standards such as IEC 60664-1 [58], reduces the touch voltage during a single pole-to-ground fault [59], and also lowers the voltage stress at the input of the PSUs. Although the midpoint can, in principle, improve grounding and fault isolation, realizing those benefits typically necessitates specialized protection hardware such as three-pole breakers [52]. Because such components are not broadly available, relying on them can increase engineering effort and create deployment delays. In addition, the three-wire arrangement complicates grounding, fault detection, and phase balancing when extended to data center scale distribution [9].

Among these drawbacks, phase balancing deserves attention, because it is inherent to bipolar operation. When the two poles carry unequal loads, their voltages tend to drift apart. To solve this problem, early bipolar LVDC microgrid systems relied on a dedicated voltage balancer to keep the system stable [60]. This balancer is commonly a half-bridge buck–boost stage whose inductor connects to the midpoint wire, redistributing current between the poles so that both pole voltages stay equal under imbalance [60], [61]. It is, however, an extra conversion stage. Its switch and inductor must be rated for the worst-case imbalance, which adds volume, losses, cost, and control complexity, and its correction range is ultimately capped by those ratings [61], [62]. A broad review of balancing architectures is given in [62], and balancer topologies are analyzed in [61]. Overall, the specialized protection hardware and the added balancing stage make the ±400 VDC bus less attractive, while the 800 VDC architecture works with widely available two-pole breakers and avoids pole load balancing concerns.

The future long-term candidate for the busbar voltage is 1500 VDC [6]. It is already established in other domains and is commonly used in applications such as solar [32], [33], [34], [35] and rail [63], [64], [65], [66], [67] to improve power delivery efficiency and reduce copper usage at high power levels. Standards such as NEC Article 690 (photovoltaic systems) and IEC 62477-1 (industrial converter environments) are often referenced in connection with this voltage class. Compared with 800 VDC, the main appeal of 1500 VDC is a further reduction in current for the same delivered power. As shown in Table 1, 1500 VDC transmits more power than

800 VDC through the same conductor cross-section under identical current constraints, which further reduces copper usage, cable count, and resistive losses, and makes this voltage attractive for very large facilities with long distribution runs.

However, bringing 1500 VDC into IT racks introduces significant challenges compared with 800 VDC. At this voltage level, standards for IT and indoor environments remain under development, and suitable components are limited. In addition, according to IEC 60664-1, the required clearance and creepage distances grow with the working voltage, and part of the copper saving of the higher voltage is therefore traded for bulkier insulation [58]. Furthermore, semiconductor availability is another drawback of the 1500 VDC system. For the PSU front end, the 1200 V SiC MOSFETs suited to the 800 VDC bus are broadly available today, whereas devices rated above 1500 V are still scarce. Hence, 1500-V designs typically resort to input-series structures built from lower-voltage devices, which adds complexity. For these reasons, 1500 VDC is viewed as a longer-term option for very large AI facilities, while 800 VDC remains a near-term solution.

III. LLC DCX RESONANT CONVERTER

In the 800 VDC architecture, the intermediate bus voltage can be unregulated since the downstream DC–DC VRMs can take care of the voltage regulation and provide regulated DC voltage to power the GPUs [68]. This feature helps the 800 VDC to 48 VDC LLC converter operate in the DC transformer (DCX) mode [68], [69], [70]. All converter candidates reviewed in this paper for the PSU stage belong to the LLC resonant family and are typically operated in DCX mode. This section therefore overviews the operating principle, governing equations, and design considerations of the LLC converter in this mode.

A. PRINCIPLES OF OPERATION

The schematic of an LLC resonant converter with a half-bridge primary side and a full-bridge secondary side is shown in Fig. 6. The primary bridge converts the input voltage V_{in} into a square-wave voltage v_{pri}, alternating between 0 and V_{in}, that excites the resonant tank formed by the resonant capacitor C_r, the series resonant inductor L_r, and the transformer magnetizing inductance L_m. The transformer, with a turns ratio of $n = N_1/N_2$, provides both the required voltage conversion ratio and isolation. The secondary bridge rectifies the transformer secondary-side voltage into the output voltage V_{out}. The series resonant frequency is:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

Using the first harmonic approximation (FHA), the rectifier and the load can be modeled as an equivalent AC resistance:

$$R_{ac} = \frac{8}{\pi^2} n^2 R_{out} \tag{2}$$

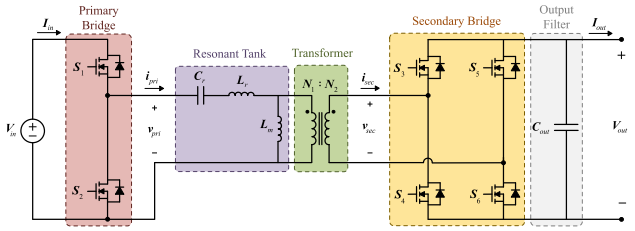


FIGURE 6. Asymmetric half-bridge LLC resonant converter.

Therefore, the normalized voltage gain of the converter, defined as $M = 2nV_{out}/V_{in}$, is [71], [72], [73]:

$$M = \frac{1}{\sqrt{\left(1 + \frac{1}{L_n}\left(1 - \left(\frac{1}{F_n}\right)^2\right)\right)^2 + Q_e^2\left(F_n - \frac{1}{F_n}\right)^2}} \tag{3}$$

where:

$$F_n = \frac{f_s}{f_r} \tag{4}$$

$$L_n = \frac{L_m}{L_r} \tag{5}$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{6}$$

And F_n is the normalized switching frequency, and Q_e is the quality factor. Unlike the conventional LLC converter that regulates the output voltage by varying the switching frequency (f_s), the LLC DCX is intended to operate at or near the resonant frequency (f_r). Hence, the resonant tank's voltage gain is nearly constant and less dependent on the load [68], [70]. As a result, the converter behaves like a DC transformer with an approximately fixed conversion ratio, which is why it is referred to as a DC transformer [74]. Equation (3) shows that at $F_n = 1$ the gain is unity regardless of Q_e, and the DCX output voltage is therefore fixed at:

$$V_{out} = \frac{V_{in}}{2n} \tag{7}$$

Fig. 7 shows the converter gain versus normalized frequency for $L_n = 10$ and different Q_e values. All curves intersect at the load-independent point $(F_n, M) = (1, 1)$, which is the DCX operating point.

Because in this mode the resonant tank input impedance is inductive, zero voltage switching (ZVS) is achieved in the primary switches at turn-on, and the synchronous rectifiers (SRs) achieve zero current switching (ZCS) at turn-off, which helps reduce switching losses [70]. The voltage stress of each primary switch is V_{in}, and, since each switch conducts the resonant tank current i_{pri} for half of the switching period, the rms current of each switch is [74]:

$$I_{sw,rms} = \frac{I_{pri,rms}}{\sqrt{2}} = \sqrt{\left(\frac{\pi I_{out}}{4n}\right)^2 + \left(\frac{nV_{out}}{8f_r L_m}\right)^2} \tag{8}$$

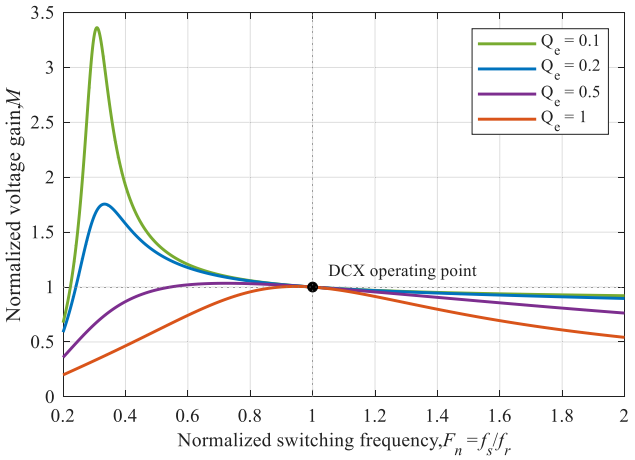


FIGURE 7. Normalized voltage gain of the LLC resonant converter versus normalized switching frequency, for $L_n = 10$ and different Q_e values.

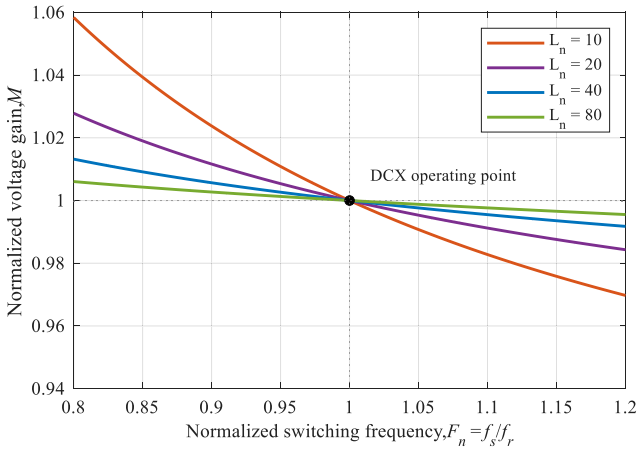


FIGURE 8. Normalized voltage gain of the LLC resonant converter versus normalized switching frequency around the DCX operating point, for $Q_e = 0.1$ and different L_n values.

B. CIRCUIT DESIGN CONSIDERATIONS

The L_n and Q_e values are the primary design parameters that govern DCX performance. A large L_n and a small Q_e are generally preferred, as this design flattens the gain characteristic around $F_n = 1$, so the DCX conversion ratio remains insensitive to load changes and to tolerance-induced mismatch between f_s and f_r [73], [74]. Fig. 8 illustrates the gain characteristic around the DCX operating point for $Q_e = 0.1$ and different L_n values. It can be observed that as L_n increases, the curve becomes progressively flatter, confirming this design principle. In addition, since a larger L_m reduces the circulating magnetizing current, it lowers both the conduction loss and the switch turn-off loss as the efficiency benefit comes primarily from a large magnetizing inductance [74], [75]. Furthermore, the small L_r allows the transformer leakage inductance to realize the entire resonant inductance, eliminating the discrete resonant inductor and its associated loss and volume [76]. These parameters cannot, however, be pushed arbitrarily far. The L_m value is bounded above by the ZVS condition:

$$L_m \leq \frac{t_d}{16 f_r C_{oss}} \tag{9}$$

where C_{oss} is the charge-equivalent output capacitance of each primary-side switch and t_d is the dead time between the primary-side switches. Compensating a violation with a longer dead time increases body-diode conduction and shortens the power-transfer interval. Likewise, a very small Q_e implies a low tank impedance, which weakens the converter's inherent current limiting under overload.

Because the PSU output current is high, SRs are used instead of diodes on the secondary side, since their low on-resistance substantially reduces rectifier conduction loss and improves overall efficiency [77], [78]. To drive SRs in the DCX mode, the same driving signal can be applied to both the primary switches and the SRs [78]. However, when f_s deviates from f_r, this shared timing mistimes the SR turn-on and turn-off instants, causing body-diode conduction or reverse current issues that result in reduced converter efficiency [78]. These turn-on and turn-off issues are analyzed in [78].

In DCX mode, component tolerances and parasitic elements, defined as the parasitic capacitance C_{par}, and the stray inductance L_{str}, shift the actual resonant point away from the intended design target [79]. The real resonant frequency can be identified either by extracting it from the resonant waveforms observed on the oscilloscope or by measuring the parasitics directly. Considering these parasitics and the pause in power transfer during the dead time, the optimum switching frequency becomes [79], [80]:

$$f_{s,opt} = \frac{1}{2\pi\sqrt{(L_r + L_{str})\left(C_r + C_{par}\right)} + 2t_d} \tag{10}$$

To lock the switching frequency to the actual resonant point, resonant frequency tracking techniques, such as the pulsewidth locked loop of [79] and the adaptive SR-based tuning of [80], can be adopted.

Because output voltage regulation is not required in DCX mode, the DCX can be operated with open-loop control at a predefined switching frequency without a fast real-time control loop, unlike the conventional LLC converter, which requires closed-loop regulation [68]. This also reduces control and sensing complexity, since high-speed ADC sampling and cycle-by-cycle control execution are not required, and only slower monitoring may be needed for high-level protection functions [68].

IV. MAGNETIC DESIGN OF THE LLC DCX CONVERTER

The magnetic design of the LLC DCX converter needs careful attention because of its role in the loss and volume of the converter. The 800 VDC to 48 VDC stage is demanding in this respect for three reasons. First, the conversion ratio requires a large transformer turns ratio. Since the required clearance and creepage distances grow with the working voltage, the

number of primary turns, the number of PCB layers, and the interwinding spacing all increase. Second, the output current of a multi-kilowatt converter at 48 VDC reaches hundreds of amperes. As a result, the secondary-side winding loss, the termination loss, and the current sharing among the paralleled SRs dominate the transformer loss. Third, the megahertz-class switching frequencies enabled by GaN devices push the magnetics toward planar PCB windings, in which core loss, fringing loss, and eddy-current loss must be controlled. This section discusses the magnetic design considerations for these converters, and reviews possible solutions for resonant inductance and transformer implementation for this application.

A. MAGNETIC DESIGN CONSIDERATIONS

Magnetic design largely determines the efficiency and power density of LLC converters, since the transformer alone contributes a sizable share of the total loss and occupies a notable part of the converter volume [81]. Operating at hundreds of kilohertz with wide-bandgap devices has resulted in the traditional labor-intensive Litz-wire magnetics being replaced by planar PCB windings. This replacement offers fully automated low-cost assembly, a low profile, repeatable parasitics, and an improved thermal surface-to-body ratio [81], [82]. However, high frequency and high power density introduce several challenges. Delivering kilowatts at a 48–54 VDC output requires many paralleled SR devices, which leads to unbalanced current sharing and high termination losses that are further magnified by the AC resistance of the PCB traces at high frequency [81], [82]. The same high output current also motivates dividing the output into several paralleled secondaries, so that the conduction loss is shared among the secondary windings and the SR devices. Once the output is paralleled in this way, the transformer winding loss, the SR switching and conduction loss, and the termination loss at the power connections can no longer be minimized independently, and a careful tradeoff must be managed among them [69].

Furthermore, PCB-wound resonant inductors suffer from severe MMF build-up between stacked layers [82]. In addition, eddy-current losses in the core become significant under high volt-second excitation [83], and the large interwinding capacitance of PCB magnetics injects common-mode noise [81], [84].

The matrix transformer has emerged as the principal solution. The single transformer is divided into elemental transformers whose primaries are connected in series and whose secondaries feed distributed rectifiers. In this way, each SR set carries only a fraction of the output power, termination loss is reduced, current sharing is guaranteed by symmetry, and heat is spread over a larger area [81], [82]. Splitting the transformer is not free, however, since several separate cores occupy a larger footprint and a larger total magnetic volume, which in turn raises the core loss [69]. By using an even number of elemental transformers with alternating

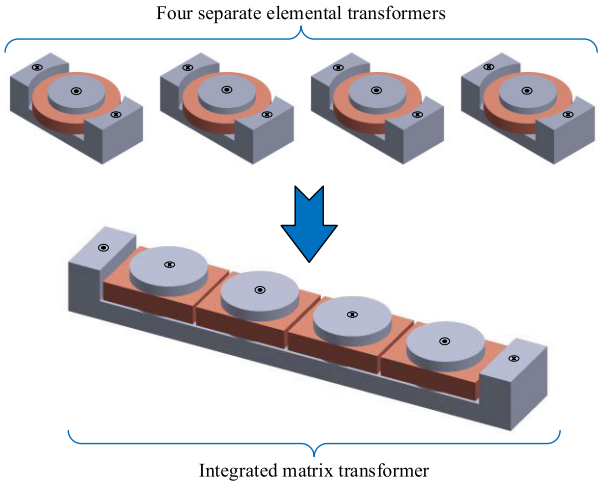


FIGURE 9. A matrix transformer implemented as four separate elemental transformer cores and a single integrated core using the flux-cancellation concept.

flux directions, the fluxes cancel in the shared legs. This allows all cores to be merged into a single multi-leg structure with reduced footprint and plate flux density, as shown in Fig. 9 [81]. Flux cancellation is therefore what allows the matrix transformer to retain the termination-loss and current-sharing benefits of subdivision while avoiding much of the footprint and core-volume penalty that separate cores would impose [69]. The 6 kW, 800 V/50 V module in [83] applies this concept by integrating two EI-core transformers into one four-leg core. The same philosophy can be applied to the resonant inductor. A matrix of elemental inductors reduces the PCB winding resistance, distributes the air gap, cuts the stray capacitance, and lowers the temperature rise [81], [82]. Going one step further, the transformer and inductor can be merged. Unbalancing the turns between elemental transformers, together with an auxiliary core leg, creates a controlled leakage inductance that realizes L_r [84], [85].

Magnetic design usually proceeds through a systematic optimization. The transformer loss separates into a load-independent fixed part (core loss plus magnetizing-current loss, constant under DCX operation) and a conduction part proportional to the square of the output current. Peak efficiency occurs where the two are equal, so the full-load conduction loss should be about four times the fixed loss. This places the efficiency peak near half load, where servers operate most of the time [81]. The winding width, core cross-section, leg elongation, and footprint are swept to the knee of the loss–footprint tradeoff [81], [83]. The ferrite material is selected by its performance factor at the target frequency, and the switching frequency itself is optimized with the combined loss reaching a minimum at the optimal frequency [81], [82]. This minimum exists because the two dominant trends act in opposite directions. A higher switching frequency reduces the size and the loss of the magnetic components, whereas the termination loss tends to grow as the current and interconnect

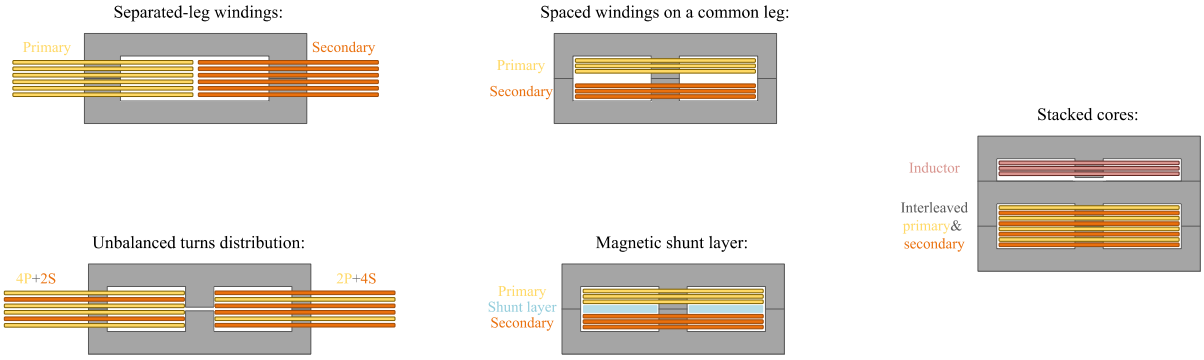


FIGURE 10. Integration methods for the inductor–transformer implementation for realizing the transformer leakage inductance as the resonant inductance.

demands at the secondary side increase [69]. The magnetizing inductance is chosen at the valley of the total device loss, since a small L_m raises the circulating current while an excessively large one lengthens the dead time and the SR discontinuous interval [83].

Finally, thermal and form factor constraints shape the final magnetic design, since modern GPU server racks are now equipped with liquid-cooling infrastructure to manage the thermal dissipation of high-power computing chips. This cooling system imposes new design constraints, as all heat-dissipating components, including power devices, must be mounted exclusively on the top side of the PCB to interface with shared cold plates [83]. This requirement, combined with the limited profile and the need for optimized SR termination, introduces considerable trade-offs in both layout and thermal–electrical co-design of the converter [83].

B. RESONANT INDUCTOR AND TRANSFORMER IMPLEMENTATION

Since the LLC DCX converter used for the 800 VDC to 48 VDC stage in AI data centers has a large L_n, the required value of L_r is usually small. The discrete resonant inductor is therefore a candidate for elimination. Realizing L_r through the leakage inductance of the transformer, L_{lk}, is referred to as inductor–transformer integration, and the resulting component is an integrated inductor–transformer [86]. The motivation is threefold. First, the magnetic components are responsible for a large share of the total loss of isolated DC–DC converters, reported to be about 40% on average over the literature [86]. The discrete resonant inductor contributes its own core loss, winding loss, and termination loss to this share. Second, magnetic scaling laws indicate that a single larger magnetic structure has a higher upper bound of achievable efficiency and power density than several smaller structures [87]. Third, the removal of the inductor eliminates one component from the bill of material and one termination from the high-current path. This is valuable in the low-profile, top-side-mounted layout imposed by the liquid-cooled racks discussed earlier.

Integration is, however, not unconditionally beneficial. Comparisons between optimized discrete and integrated magnetics have reached opposite conclusions depending on the operating conditions [88], [89]. The benefit therefore depends on the integration method, on the required inductance value, and on the power level. Hence, the method must be selected with care. In all cases, the series inductance is obtained by deliberately controlling the leakage inductance of the transformer, that is, the flux that links one winding without linking the other. The design problem is to provide a well-defined, repeatable, and low-loss path for this decoupled flux. Five integration methods can be distinguished [86]. They are illustrated in Fig. 10 and are described below:

1) SEPARATED-LEG WINDINGS

The primary and the secondary windings are placed on different legs of the core, for example on the two legs of a UI-core. In this way, the two windings share only the flux circulating in the core, while the decoupled flux closes through the surrounding air. Because the decoupled flux path is long and lies partly outside the core, this arrangement provides the largest leakage inductance of the five methods. Values of hundreds of microhenries are reached with a few tens of turns per winding [90], [91]. The value is set by the number of turns and by the core and winding geometry [90], [91]. The arrangement is attractive for PCB windings because each core window carries only one winding, which doubles the number of turns available per layer. It has been applied from kilowatt-class DC–DC stages [90], [91], [92], [93] to medium-frequency transformers in the hundred-kilowatt and megawatt range [94], [95]. Its main drawback is that the primary and secondary windings cannot be interleaved, so that the AC winding loss at high frequency is elevated. In addition, the decoupled flux in the air induces eddy currents in nearby conductors, raises the radiated EMI, and enlarges the footprint compared with a conventional transformer.

2) SPACED WINDINGS ON A COMMON LEG

The primary and the secondary windings are wound on the same core leg but are separated axially by a gap. The decoupled flux is stored in this gap. The leakage inductance increases with the number of turns, with the winding width, and with the winding separation. In this way, it is tuned

TABLE 2. Comparison of the magnetic integration methods.

Feature	Separated-leg windings	Spaced windings on a common leg	Magnetic shunt layer	Stacked cores	Unbalanced turns distribution
Path of the decoupled flux	Air surrounding the core, between separate legs	Gap between axially separated windings on a common leg	Magnetic layer inserted between the windings	Dedicated inductor legs with air gap; shared core plates	transformer central leg with partial flux cancellation
Parameter setting L_r	Turns, leg and winding geometry	Winding separation	Shunt thickness, permeability, and gap	Inductor air gap	Turn imbalance and central-leg gap
Achievable inductance	Highest; hundreds of µH with a few tens of turns	Lowest; a few µH to a few tens of µH	High; a few µH to a few hundred µH	Widest range; a fraction of a µH to tens of µH	High; approximately 1 µH to 10 µH
Power density	Low; footprint larger than a conventional transformer	Moderate; added winding height	Moderate; shunt adds height and loss	Highest volumetric power density	Highest surface power density
Design simplicity	Moderate; air-path leakage depends on surroundings	High; one-dimensional field, analytical models	High; reluctance model of the gaps	High; inductor gap tuned independently of the transformer	Low; magnetizing and leakage inductances interdependent
PCB suitability	Good; one winding per window, twice the turns per layer	Poor; requires winding height	Moderate; shunt sheet or leg between layers	Good; interleaved PCB windings retained	Good; split PCB windings halve the layer count
Manufacturability	Good; standard core shapes	Moderate; suited to wire-wound magnetics	Poor; custom core or embedded material	Good; custom cores, more terminations	Good; EI cores with a gapped central leg
EMI performance	Poor; leakage field radiates through air	Moderate; flux within the core window	Good; flux guided by the shunt	Good; flux in dedicated legs	Best; flux confined in the central leg
Representative implementations	[90]–[95]	[97]–[100]	[101]–[108]	[109]–[116]	[117]–[126]

simply by the distance between the windings. Because the field between two separated winding blocks is nearly one-dimensional, the leakage inductance can be estimated accurately with classical analytical winding models [96]. This makes it the easiest method to design and to model. The achievable inductance for a given volume is the lowest of the five methods, and the reported values range from a few microhenries to a few tens of microhenries [97], [98], [99], [100]. The separation of the windings, however, requires winding height. This is unfavorable for low-profile planar magnetics and limits the suitability of the method for PCB implementation for AI data centers. Furthermore, the two winding blocks are not interleaved, so that the AC winding loss is higher than in an interleaved transformer.

3) MAGNETIC SHUNT LAYER

The spaced winding method is extended by inserting a layer of magnetic material, the shunt, between the primary and the secondary windings. The shunt provides a low-reluctance path for the decoupled flux, so that the leakage inductance is substantially increased for the same winding separation [101], [102], [103], [104]. The value is set by the thickness, the permeability, and the air gaps of the shunt layer. The shunt can be a leg of a custom core or a sheet of magnetic material inserted between the PCB layers. The latter suffers from additional core loss and from permeability variations caused by manufacturing tolerances and temperature [103], [105]. Segmented shunts allow the leakage and magnetizing inductances to be tuned independently [106], and separate shunts for the primary and the secondary windings provide different leakage values on the two sides [107]. In addition, extended ferrite plates with distributed air gaps can serve as shunts while reducing the fringing loss [108]. Its power density and manufacturability are the weakest among the five methods [86].

4) STACKED CORES

The inductor keeps its own winding and its own core legs. The two magnetic structures are stacked vertically or horizontally so that they share part of the core plates [109], [110], [111], [112], [113], [114], [115], [116]. Since the transformer flux and the inductor flux are shifted in phase, the flux density in the shared core sections is lower than the sum of the two. As a result, the shared plates can be smaller than those of the separate components. The inductance is set by the air gap of the inductor legs, so that it can be tuned independently of the transformer over a very wide range, from a fraction of a microhenry to tens of microhenries. It is the most frequently used integration method and has achieved the highest volumetric power densities among integrated magnetics [86]. Its main drawback is that custom core shapes are generally required. In addition, vertically stacked structures built from several PCBs complicate the board-to-board connections and terminations.

5) UNBALANCED TURNS DISTRIBUTION

This method starts from the matrix transformer of two elemental transformers with split PCB windings that share the central leg of an EI-core [117]. In the balanced case, the fluxes of the two elements cancel in the central leg. The primary and

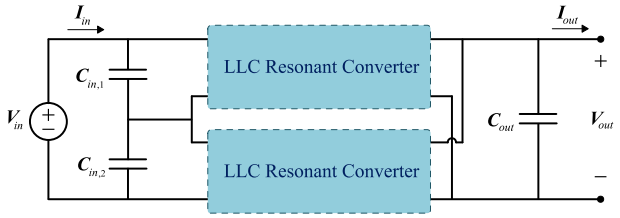


FIGURE 11. Input-series output-parallel LLC resonant converter.

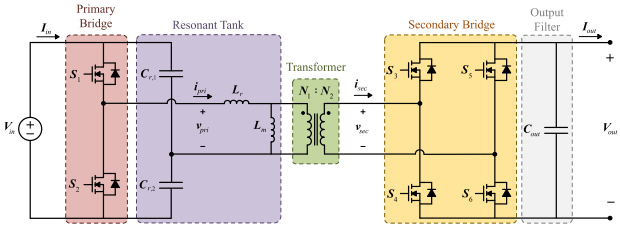


FIGURE 12. Symmetric half-bridge LLC resonant converter.

secondary turns are then distributed unequally between the two elemental transformers, for example with the majority of the primary turns on one element and the majority of the secondary turns on the other. In this case, the cancellation in the central leg is only partial, and the residual flux in the central leg constitutes the leakage inductance. The value is controlled by the number of turns, by the degree of unbalance, by the air gap of the central leg, and by its geometry [118], [119], [120], [121], [122], [123], [124]. Since the decoupled flux is confined within a dedicated core leg, the windings can be largely interleaved and the flux does not radiate into the surroundings. As a result, both the AC winding loss and the EMI are low. When extended to three-phase matrix transformers, the 120-degree phase shift among the phases makes the central-leg flux vanish, so that the central leg can be removed. This also removes the possibility of tuning the leakage independently of the magnetizing inductance through the central-leg gap [125], [126].

The requirements of the 800 VDC to 48 VDC DCX stage favor integration and the realization of L_r as transformer leakage inductance. The required L_r is small. In addition, no frequency modulation is used, so that a large leakage inductance is not needed to shape the gain characteristic. Consequently, the selection among the five methods for this stage is governed by the winding loss, the profile, and the compatibility with the planar matrix structure rather than by the achievable inductance. This favors the stacked-core and unbalanced-turns methods.

The disadvantages of integration for this application are the loss of independent optimization and the sensitivity of the leakage inductance value. In an integrated structure, the magnetizing inductance, the leakage inductance, the core loss, and the thermal path are coupled. As a result, the design space is more constrained and the optimization is more difficult than for separate components [88], [89]. Because the leakage inductance is determined by the winding geometry and by the air gaps, its tolerance is larger than that of a discrete inductor. The resulting spread of the resonant frequency is a particular concern for the DCX, which is operated open-loop at a fixed switching frequency. It is also a concern for the modular and multiphase structures reviewed in the following sections, whose current sharing depends on the matching of the resonant tanks. Furthermore, thermal management becomes more difficult, since the losses of the inductor and of the transformer are concentrated in one component. Finally, most integration methods rely on custom core shapes, which increases the tooling cost and lengthens the development time. Table 2 summarizes the five integration methods in different terms [86].

V. HALF-BRIDGE LLC RESONANT CONVERTER

One of the most widely used topologies for the isolated DC–DC conversion stage in AI data centers is the half-bridge LLC topology, shown in Fig. 6. In the existing 48 VDC data center architecture, this topology has been extensively adopted as the 400 VDC to 48 VDC conversion stage in 480 VAC-input, 48 VDC-output PSUs. It has been investigated in several works, including [81], [82], [84], [85], and [127]. In particular, considerable efforts have been directed toward improving the magnetic design and integration of this converter to increase efficiency and power density. For example, in [81], a 3 kW, 400 VDC to 48 VDC LLC converter is demonstrated, in which a four-transformer matrix is used to distribute the secondary-side full-bridge rectifiers, and a matrix resonant inductor is introduced to reduce PCB winding loss caused by proximity effect and MMF build-up. Similarly, in [85], a 3 kW, 400 VDC to 48 VDC converter with an integrated transformer–inductor is implemented, in which an optimized EEI-core is introduced to improve leakage-flux distribution. An input-series output-parallel (ISOP) converter can also be implemented, as shown in Fig. 11, to enable the use of lower-voltage primary-side devices like GaN switches. By using GaN switches, a higher switching frequency can be achieved, which allows the transformer and surrounding components to be further miniaturized [21].

A. SYMMETRIC HALF-BRIDGE LLC CONVERTER

An extension of this topology is the split resonant capacitor version, whose geometry is shown in Fig. 12. It has been used for the isolated 400 VDC to 48 VDC conversion stage of data center PSUs in [128] and [129]. This topology, also referred to as the symmetric half-bridge LLC topology, is a practical variant of the conventional half-bridge LLC topology, which may also be referred to as the asymmetric half-bridge LLC topology. In the symmetric topology, the single resonant capacitor C_r is replaced by two capacitors, $C_{r,1}$ and $C_{r,2}$, each of which is equal to $C_r/2$. Because $C_{r,1}$ and $C_{r,2}$ are dynamically in parallel, the equivalent resonant capacitance seen by the tank remains equal to C_r [130]. This topology should not be regarded as a different resonant family, but

TABLE 3. Comparison of the asymmetric and symmetric half-bridge LLC topologies.

Aspect	Asymmetric HB LLC	Symmetric HB LLC
Primary switch voltage stress	V_{in}	V_{in}
Primary switch RMS current	$\frac{I_{pri,rms}}{\sqrt{2}}$, as in (8)	$\frac{I_{pri,rms}}{\sqrt{2}}$, as in (8)
DC bias voltage per resonant capacitor	$V_{cr} = V_{in}/2$	$V_{cr,1} = V_{cr,2} = V_{in}/2$
ZVS and ZCS behavior	ZVS on primary, ZCS on SRs	Identical
RMS current per resonant capacitor	Full $I_{pri,rms}$ through C_r	$I_{pri,rms}/2$ through $C_{r,1}$ and $C_{r,2}$
Input current waveform	Pulsating (drawn during high-side conduction)	Continuous (drawn in both half-cycles)
Bus-capacitor ripple demand	Higher rms ripple	Lower rms ripple, reduced diff.-mode noise
Typical preference	Lower power, minimum part count	Higher power, better input current waveform

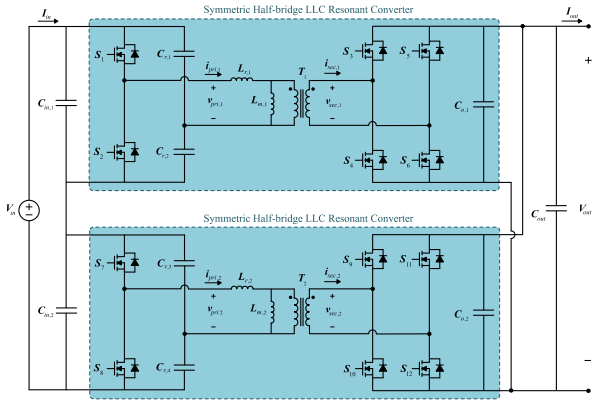


FIGURE 13. Input-series output-parallel symmetric half-bridge LLC resonant converter.

rather as another implementation of the same half-bridge LLC resonant tank. As a result, the resonant-circuit analysis and the usual design concepts for frequency-dependent gain, resonance, and soft switching remain the same as in the asymmetric half-bridge LLC [131]. Consequently, the semiconductor stresses are also identical in the two versions. Each primary switch blocks the full input voltage and conducts the same resonant tank current for half of the switching period, so both the peak voltage stress and the rms current stress of the primary switches are unchanged [130].

The main difference between the symmetric and asymmetric topologies lies in the physical implementation of the resonant capacitance and in the resulting current-stress distribution. Table 3 shows the comparison of the asymmetric and symmetric half-bridge LLC topologies in different aspects. In the asymmetric topology, the single C_r is connected in series with L_r, and it not only participates in resonance but also provides the dc-blocking function [130]. In the symmetric topology, the same total resonant capacitance is realized by two capacitors, and the resonant current is shared between them, so the current stress in each capacitor is reduced [132]. In addition, the split-capacitor arrangement modifies the input-current waveform, making it continuous and closer to the input current of a full-bridge converter [130], which also lowers the rms ripple-current demand on the input bus capacitor [132]. The start-up behavior differs as well. In the asymmetric topology, C_r is initially discharged, which can cause an initial volt-second imbalance across the transformer during the first switching cycles, whereas in the symmetric topology each capacitor is pre-biased near $0.5V_{in}$, resulting in a milder start-up transient [130], [132]. These features are beneficial at higher power levels and for reducing differential-mode noise [130]. From a practical point of view, the symmetric topology is mainly adopted for higher-power applications and when the benefits of lower capacitor stress and improved input-current behavior justify the use of one additional capacitor. However, the asymmetric topology is more attractive when lower part count and simpler implementation are preferred. In practice, the choice between them is mainly a tradeoff between simplicity and improved stress distribution.

B. AI DATA CENTER DESIGNS

Among the candidate realizations for 800 VDC to 48 VDC converters in AI data centers, the ISOP symmetric half-bridge LLC topology has been introduced as a solution in [68], [133], [134], and [135]. This configuration is attractive because connecting the LLC modules in input-series form divides the input voltage among the modules, thereby reducing the voltage stress on the primary-side switches and enabling the use of devices with lower voltage ratings and better switching performance. For example, in [136] and [137], a 12 kW, 1 MHz, 800 VDC to 50 VDC converter is implemented by paralleling two 6 kW converters. In each 6 kW converter, as shown in Fig. 13, two LLC modules, each powered by 400 VDC (half of the 800 VDC bus), are connected in input-series and output-parallel form. Using this arrangement, the voltage stress of the primary-side devices is $0.5V_{in}$. In addition, a matrix transformer is adopted to enable flux cancellation, thereby reducing the core size and improving load sharing among the elemental transformers. In [138], an 11 kW, 800 VDC to 50 VDC converter is reported, and its implementation is demonstrated using four 2.75 kW, 200 VDC to 50 VDC modules, where each module is an ISOP converter composed of two 100 VDC to 50 VDC symmetric half-bridge LLC modules. Similarly, in [83], a 6 kW, 615 kHz, 800 VDC to 50 VDC LLC converter is implemented using two 3 kW half-bridge LLC modules, where two EI-core transformers are integrated into a single four-leg core. To further improve output-side current ripple performance, an interleaved version of the same topology has also been investigated. In [139], an interleaved ISOP symmetric half-bridge LLC resonant converter is introduced, where a 90-degree phase shift in the primary-side switch timing is used to reduce

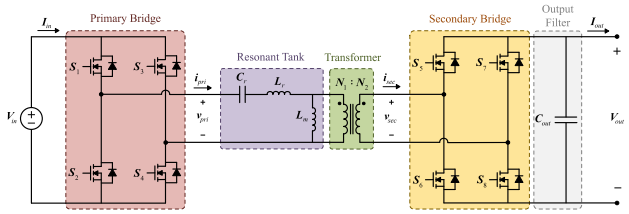


FIGURE 14. Full-bridge LLC resonant converter.

the ripple current of the output capacitor, thereby reducing the output-voltage ripple and the AC losses at the output side.

VI. FULL-BRIDGE LLC RESONANT CONVERTER

The second solution topology for the isolated DC–DC conversion stage in data center power architecture is the full-bridge LLC resonant converter, shown in Fig. 14. This topology has been proposed for the 400 VDC to 48 VDC conversion stage in [140], [141], [142], [143], and [144] for data center PSUs of the 48 VDC architecture, and several studies have investigated its implementation, including [145], [146], [147], [148], [149], [150], [151], [152], and [153]. In particular, considerable research has been directed toward improving the magnetic integration, control, and power density of this converter. For example, in [145] and [146], a 3 kW, 400 VDC to 48 VDC resonant converter is demonstrated, in which a five-leg PCB magnetic structure is proposed to embed the resonant inductor into a matrix transformer composed of four elemental transformers, while also providing controllable leakage inductance through the integrated magnetic structure. In [147], an improved synchronous-rectification LLC converter is proposed for hold-up-time operation, in which one additional secondary-side switch and a fixed-frequency phase-shift control method are used to increase voltage gain and extend the hold-up time. In [148], [149], and [150], dimensional effects in high-frequency planar magnetics, including flux crowding, dimensional resonance, core eddy loss, and termination loss, are characterized and mitigated, and their impact is verified through the design of a 1 MHz, 3 kW, 400 VDC to 48 VDC converter. In addition, [151] reviews major research directions in high-frequency LLC converters for data center applications, including advanced magnetic integration for higher power density and advanced control methods for improved transient performance.

A. FULL-BRIDGE AND SYMMETRIC HALF-BRIDGE CONVERTER COMPARISON

Table 4 compares the full-bridge LLC with the symmetric half-bridge LLC under identical operating conditions — the same output power, gain, input voltage, resonant frequency, FETs, and transformer core — showing that the full-bridge halves the primary conduction loss and copper loss at the cost of doubling the switch count [130], [154]. In the full-bridge LLC converter, considering the DCX operation and the transformer turns ratio of n = N_1/N_2, the resonant tank has

TABLE 4. Comparison of the full-bridge LLC and the symmetric half-bridge LLC topologies under identical operating conditions.

Aspect	Full-bridge LLC	Symmetric HB LLC
Number of primary switches	4	2
Primary switch voltage stress	V_{in}	V_{in}
Resonant tank excitation voltage	$\pm V_{in}$ (square wave)	$\pm V_{in}/2$ (square wave with $V_{in}/2$ DC bias)
Transformer primary turns, N_1	$2N_{1,HB}$	$N_{1,HB}$
Primary winding DC resistance R_{pri}	$2R_{pri,HB}$	$R_{pri,HB}$
Primary switch RMS current ($I_{sw,rms}$)	×0.5	1 (reference)
Total primary FET conduction loss	×0.5	1 (reference)
Total primary winding copper loss	×0.5	1 (reference)
Typical use case	High output power, high primary current	Low-to-medium power, minimum switch count

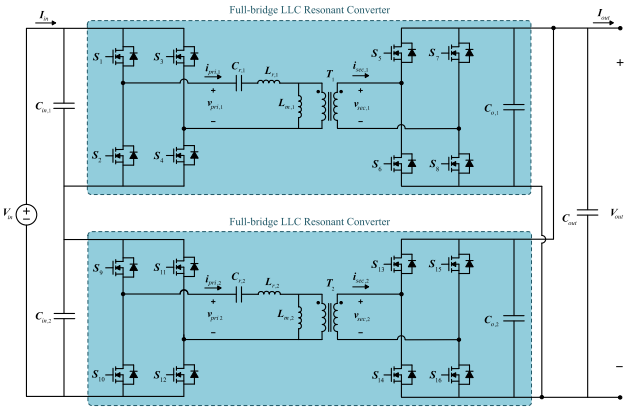


FIGURE 15. Input-series output-parallel full-bridge LLC resonant converter.

unity gain regardless of Q_e, and the converter output voltage is fixed at:

$$V_{out} = \frac{V_{in}}{n} \tag{11}$$

The voltage stress of each primary switch is V_{in}, and, since each switch pair, (S_1, S_4) and (S_2, S_3), conduct the resonant tank current i_{pri} for half of the switching period, the rms current of each switch, at the resonant frequency where the tank current is sinusoidal, is [74]:

$$I_{sw,rms} = \frac{I_{pri,rms}}{\sqrt{2}} = \sqrt{\left(\frac{\pi I_{out}}{4n}\right)^2 + \left(\frac{nV_{out}}{8f_r L_m}\right)^2} \tag{12}$$

It should be noted that, although (12) has the same form as the half-bridge expression in (8), the two do not yield the same value. Under DCX operation unity gain requires

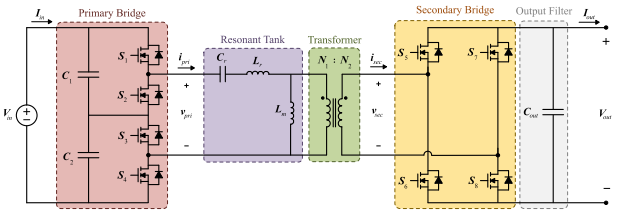


FIGURE 16. Three-level half-bridge LLC resonant converter with a full-bridge rectifier.

$nV_{out} = V_{in}$ in the full-bridge versus $2nV_{out} = V_{in}$ in the half-bridge, so the full-bridge turns ratio is twice as large. Hence, the full-bridge primary switch rms current is half that of the half-bridge for the same output power.

B. AI DATA CENTER DESIGNS

For 800 VDC to 48 VDC converters, [141], [142] indicate that a practical approach is to build the 800-V converter by stacking two 400-V converter modules, in the way that the primary sides are connected in input-series form while the secondary sides are connected in output-parallel form, as shown in Fig. 15. In this way, the split input bus allows the total input voltage to be divided between the two modules, so each module processes only half of the input voltage while the outputs of the two modules are combined at the low-voltage side. This building-block approach is attractive because it extends previously developed 400 VDC to 48 VDC converter technology to the 800 VDC bus with lower primary-side voltage stress and a modular implementation path. In this approach, the switch selection also benefits from the stacked implementation. As discussed in [141], if each LLC stage is connected across the full high-voltage bus, 1200 V primary-side devices are required, whereas connecting two LLC stages in input-series form allows the use of 650 V SiC or GaN devices on the primary side because each stage processes only half of the bus voltage.

VII. THREE-LEVEL HALF-BRIDGE LLC RESONANT CONVERTER

The third candidate topology that can be used for the 800 VDC to 48 VDC isolated DC–DC conversion stage in AI data centers is the three-level half-bridge (TLHB) LLC resonant converter. The schematic of this topology, which is also known as the series or stacked half-bridge (SHB) LLC resonant converter, is shown in Fig. 16. This topology is a resonant converter designed and well-suited for high-input-voltage (e.g., 800–1500 V) DC–DC power conversion applications. It has been introduced as a solution for the 800 VDC to 48 VDC power conversion stage for AI data centers in [69], [70], [139], and [155].

In this topology, the input voltage, V_{in}, is split by two input bus capacitors, C_1 and C_2, and each capacitor maintains about half of the input voltage ($0.5V_{in}$). Unlike the conventional half-bridge structure, the three-level half-bridge structure uses four switches, S_1–S_4, in a stacked configuration on the primary side. The two complementary switch pairs, (S_1, S_2) and (S_3, S_4), excite the resonant tank with an AC voltage, v_{pri}, that can be switched among zero, half of the input voltage, and the input voltage. The resonant capacitor, C_r, is part of the resonant tank and prevents DC voltage from being applied to the transformer primary side. On the secondary side, the full-bridge rectifier converts the AC voltage, v_{sec}, to the DC output voltage, V_{out}. The key advantage of this structure for 800 VDC applications is that each primary switch voltage stress is roughly $0.5V_{in}$, which is half of the voltage stress of the primary switches in the conventional full-bridge LLC converter with the same number of four switches. This reduced voltage stress allows the use of lower-voltage devices with faster switching capability.

A. MODULATION METHODS

Different two-level [139], [156], [157], [158] and three-level [156], [157], [158] modulation methods can be applied to the primary-side switches to generate different v_{pri} voltages for exciting the resonant tank. The two-level modulation method can be applied through the in-phase control mode or the double-frequency control mode. In the in-phase control mode shown in Fig. 17(a), the inverter stage generates v_{pri}, which is a 50% duty cycle AC voltage that alternates between 0 and V_{in}, and therefore has a DC value of $0.5V_{in}$. In this mode, the switch pairs (S_1, S_4) and (S_2, S_3) each conduct for 50% of the switching period, which results in equal conduction loss distribution among the four switches. Proper voltage balancing between C_1 and C_2 is essential for correct operation of the TLHB LLC converter; however, non-ideal effects such as line capacitance and asymmetry in the drive pulse width can gradually unbalance the voltages of C_1 and C_2 during practical operation [70], [139]. As this imbalance grows, the voltage stress on the power switches increases, which weakens the original benefit of this structure and, in severe cases, can even create a risk of switch overvoltage damage. This issue can be mitigated by adjusting the phase of the drive signals within the in-phase control mode so that the capacitor voltages remain balanced [139].

The double-frequency control mode is shown in Fig. 17(b). In this mode, the inverter generates v_{pri} as an AC voltage that alternates between 0 and $0.5V_{in}$, and therefore has a DC value of $0.25V_{in}$. Under this operating mode, switches S_2 and S_3 each conduct 75% of the switching period, whereas S_1 and S_4 each operate for 25% of the switching period. This switching pattern acts as a frequency doubler for the resonant tank, reducing switching and core losses of the converter [83]. Compared with the in-phase control mode, this operating mode applies a 0.5 step-down factor to v_{pri}, which can provide part of the converter step-down conversion ratio and reduce the required transformer turns ratio. With this control mode, even if a duty mismatch exists, the voltages of C_1 and C_2 may still exhibit a static error, but they do not continue to drift toward increasing imbalance over time [139]. However, these benefits are obtained at the cost of significantly higher and unequal conduction loss in the primary-side switches.

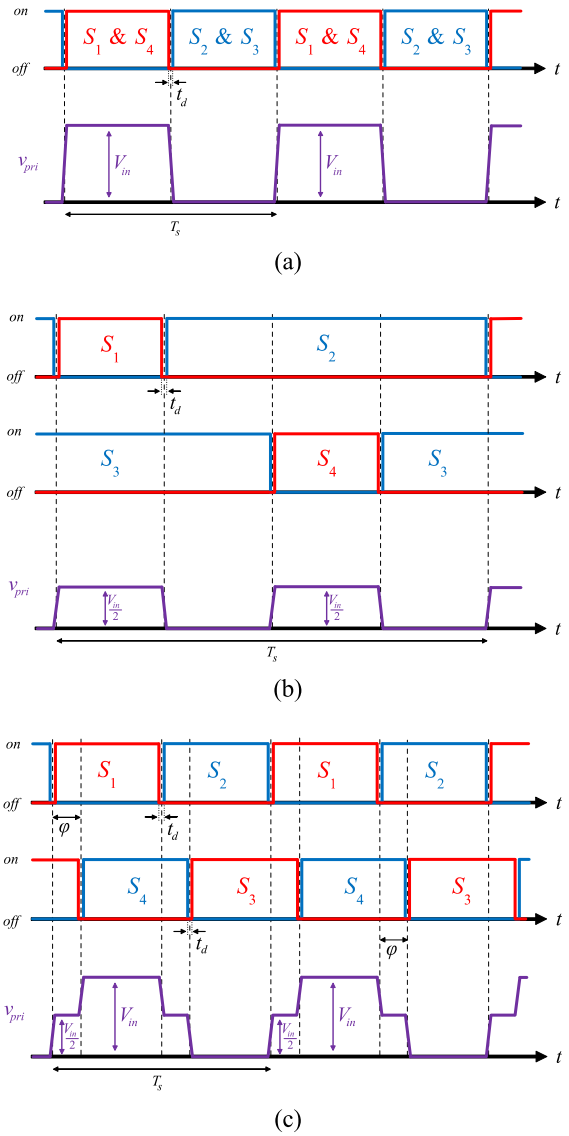


FIGURE 17. Primary-side switch gating patterns and corresponding v_{pri} waveforms for (a) in-phase control, (b) double-frequency control, and (c) three-level modulation (lag phase-shift) mode.

The three-level modulation mode is a control method in which the inverter generates v_{pri} as an AC voltage that alternates between 0, $0.5V_{in}$, and V_{in}. Different three-level modulation variants for this converter have been introduced, and their features, advantages, and drawbacks are discussed in [157] and [158]. These include the P-mode three-level modulation, the N-mode three-level modulation, and the neutral-point (NP) voltage balancing modulation in the lead phase-shift mode and the lag phase-shift mode. The lag phase-shift mode switch turn-on pattern and the generated v_{pri} waveform are shown in Fig. 17(c).

B. AI DATA CENTER DESIGNS

For AI data center applications, in [155], a 6 kW, 800 VDC to 54 VDC, three-level half-bridge LLC converter with two paralleled secondary sides is demonstrated with 99% peak efficiency, using 650 V GaN switches on the primary side and 100 V GaN switches on the secondary side. Because this topology limits the primary switches' voltage stress to half of the input voltage, 650 V GaN switches were used on the primary side, and this supported higher switching frequency operation and enabled a 1 MHz switching frequency. GaN switches offer advantages over conventional silicon MOSFETs in LLC converters because they support higher switching frequency and faster transitions with lower switching losses [70]. This enables the use of smaller magnetic components and helps to improve power density and overall efficiency. Paralleling multiple secondary sides is a practical way to reduce current stress on the secondary-side devices in this topology, and this approach is used in [69]. In [69], a 10 kW, 800 VDC to 50 VDC, three-level half-bridge LLC converter with four paralleled secondary sides is implemented. By using 650 V and 100 V GaN switches, it enabled a 1 MHz switching frequency and achieved about 98% converter peak efficiency. Beyond these AI data center prototypes, matrix transformer designs for this topology have also been reported in 800 VDC to 48 VDC converters developed for other applications, such as EVs [159], [160]. Although the end application differs, these converters share the same high step-down ratio and high secondary-side current that characterize the 800 VDC to 48 VDC stage. In particular, [160] shows that adding windings to the side legs of the matrix transformer achieves flux shunting and a more uniform flux distribution without modifying the air-gap structure of the converter, so that an off-the-shelf core with a uniform gap can be used.

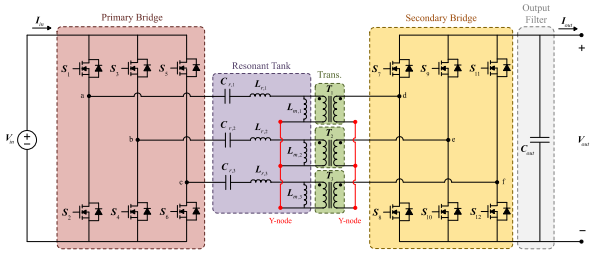


FIGURE 18. Three-phase LLC resonant converter with Y-primary and Y-secondary transformer connections.

VIII. THREE-PHASE LLC RESONANT CONVERTER

Another topology that can be used for the isolated 800 VDC to 48 VDC conversion stage in AI data centers is the three-phase LLC resonant converter in DCX mode, which has been reported in [21], [70], and [161] as a solution for this application. This topology is suitable for high-power and high-current applications.

The circuit schematic of the three-phase LLC converter with Y-primary and Y-secondary transformer connections, presented in [70], is shown in Fig. 18. In this topology, the three-phase operation allows the total power to be distributed among three phases and three resonant tanks, thereby reducing the current stress of the resonant tank elements and

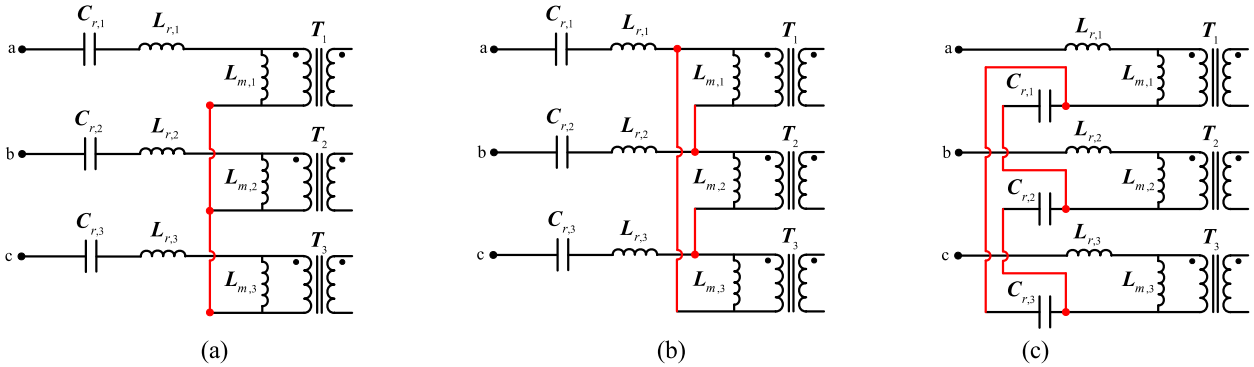


FIGURE 19. Transformer primary-side connections in the three-phase LLC resonant converter: (a) Y-Primary connection, (b) Δ-Primary connection, and (c) primary Δ-C_r network.

bridge switches. In addition, the output ripple frequency is six times the switching frequency, which helps reduce the output ripple current, lower the required output filter capacitance, and improve power density [70]. However, despite the advantages of this topology, it requires three separate capacitors, inductors, and transformers, which increases system volume and cost [162]. Therefore, magnetic integration is needed to reduce the converter size at the expense of increased design and manufacturing complexity [163]. Compared with conventional half-bridge and full-bridge LLC resonant converters, the three-phase LLC topology is more suitable for power levels above 10 kW [70].

A. TRANSFORMER AND RESONANT TANK CONNECTIONS

Different topologies have been proposed for the three-phase LLC converter. These topologies provide different tradeoffs between transformer winding loss and core loss, which allow the magnetic design to be better optimized [70]. This is important because magnetic component design is among the main challenges in achieving high efficiency and high power density. There are different options for interconnecting the primary side. These include the Y-Primary connection [164], in which the transformer primary sides are connected to a common Y-node, the Δ-Primary connection [165], and the primary Δ-C_r network [166], in which a delta-connected resonant capacitor network is employed on the primary side. There are also different options for interconnecting the secondary side, including the Y-Secondary connection [167], in which the transformer secondary sides are connected to a common Y-node, and the Δ-Secondary connection [168]. These primary- and secondary-side interconnection options are depicted in Fig. 19 and Fig. 20 respectively. Table 5 compares the features of different three-phase primary-side and secondary-side structures. Here, I_{pri} and I_{sec} denote the primary and secondary phase-leg currents, $I_{tx,pri}$ and $I_{tx,sec}$ the transformer primary and secondary winding currents, and $V_{tx,pri}$ and $V_{tx,sec}$ the voltages across the transformer primary and secondary windings at the resonant frequency. Compared with the transformer Y-type connection, the transformer Δ-type connection generally reduces transformer winding loss

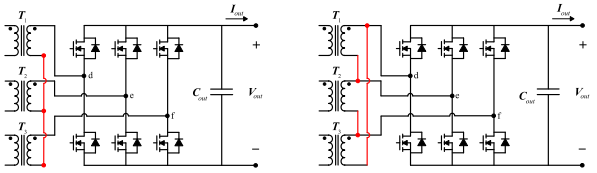


FIGURE 20. Transformer secondary-side connections in the three-phase LLC resonant converter: (a) Y-Secondary connection, and (b) Δ-Secondary connection.

TABLE 5. Comparison of different three-phase connections.

Structure	Transformer Voltage	Transformer Current
Y-primary	$V_{tx,pri} = V_{in}/2$	$I_{tx,pri} = I_{pri}$
Δ-primary	$V_{tx,pri} = \sqrt{3}V_{in}/2$	$I_{tx,pri} = I_{pri}/\sqrt{3}$
Δ-C_r Network	$V_{tx,pri} = V_{in}/2$	$I_{tx,pri} = I_{pri}$
Y-secondary	$V_{tx,sec} = V_{out}/2$	$I_{tx,sec} = I_{sec}$
Δ-secondary	$V_{tx,sec} = \sqrt{3}V_{out}/2$	$I_{tx,sec} = I_{sec}/\sqrt{3}$

because the current in each winding is lower. In particular, the winding current is reduced by a factor of $\sqrt{3}$, which decreases the winding loss to one-third. However, the voltage-second applied to the transformer also increases by a factor of $\sqrt{3}$. Compared with the Δ-type connection, the Y-type connection can reduce core loss because each winding is subjected to a lower voltage.

Beyond the transformer primary- and secondary-side connection options, additional topology variations can be achieved by changing the resonant tank configuration. By altering the resonant capacitors to a Δ connection, the primary Δ-C_r network is formed. Compared with Y-Primary, the resonant capacitance in the primary Δ-C_r network is reduced to one-third [169]. Moreover, unlike the Y-Primary case, where an offset voltage of $0.5V_{in}$ appears across the resonant capacitor, no offset voltage exists in the primary Δ-C_r network because the capacitor voltage is naturally offset by the voltage difference between the two transformers [169]. Similar to the Δ-C_r network, the Δ-L_r network [170] is obtained by altering the resonant inductor to a Δ

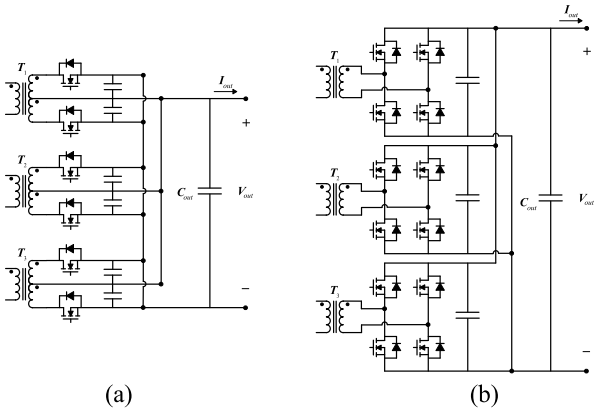


FIGURE 21. Transformer secondary-side connections in the interleaved three-phase LLC resonant converter: (a) center-tap secondary, and (b) full-bridge secondary.

connection. Likewise, the resonant inductance in the Δ-L_r network is reduced to one-third compared with Y-Primary. However, because transformer leakage inductance is usually used as part or all of the resonant inductance, this topology has limitations in the resonant-inductor connection, magnetic integration, and efficiency, and its use is not widespread [170].

B. INTERLEAVED STRUCTURES

Considering a primary-side connection from Fig. 19 together with the center-tap secondary [171] or the full-bridge secondary [171], as depicted in Fig. 21, leads to an interleaved three-phase LLC resonant converter, as described in [169]. A three-phase interleaved LLC resonant converter with the Y-primary transformer connection and the full-bridge secondary is shown in Fig. 22. The converter of Fig. 18 with Y-secondary connection and the converter of Fig. 22 with full-bridge secondary differ in several respects. The Y-secondary is rectified by a single three-phase bridge and therefore requires six SRs, whereas the full-bridge secondary requires twelve SRs and a separate output capacitor for each phase. The two configurations also excite the transformer differently. In the full-bridge secondary, each secondary winding is clamped to $\pm V_{out}$ by its own rectifier and is therefore excited by a two-level square voltage, whereas in the Y-secondary each winding is excited by the phase voltage of the three-phase rectifier, which is a six-step waveform. Two consequences follow. First, for the same input and output voltages, the Y-secondary requires twice the transformer turns ratio, i.e., 16:1 rather than 8:1 per phase in an 800 VDC to 50 VDC DCX design, which increases the number of primary turns. Second, for the same output power, the secondary winding and rectifier currents are doubled, which is a drawback for the 800 VDC to 48 VDC stage, where the high secondary-side current is already a dominant design constraint.

C. AI DATA CENTER DESIGNS

For future AI data center applications, in [21], a 20 kW, 800 VDC to 50 VDC, three-phase LLC resonant converter with

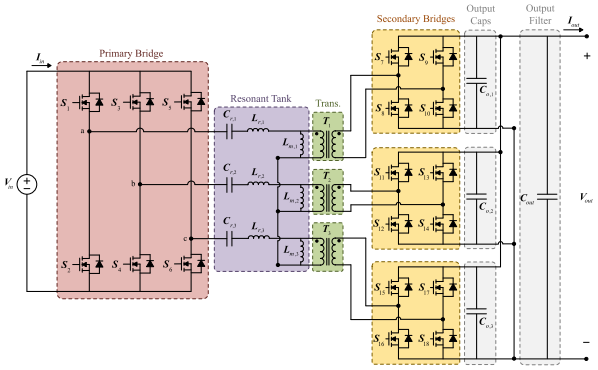


FIGURE 22. Three-phase LLC resonant converter with the Y-primary transformer connection and the full-bridge secondary.

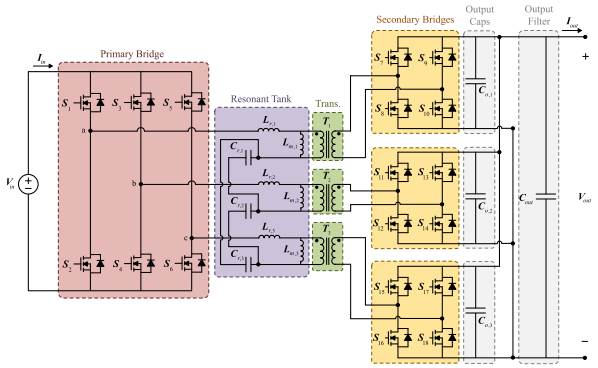


FIGURE 23. Three-phase LLC resonant converter with the primary Δ-C_r network and the full-bridge secondary.

the Y-primary transformer connection and the full-bridge secondary is implemented. It uses 1200 V SiC MOSFETs on the primary side and 80 V Si MOSFETs on the secondary side. Also, the ISOP version of this topology is proposed, which enables the use of GaN switches on the primary side. As a result, the current flowing through the primary side and the transformer is halved, which further improves efficiency. In [161], a 10 kW, 800 VDC to 54 VDC, three-phase DCX converter is implemented, and its schematic is shown in Fig. 23. The converter employs the primary Δ-C_r network and the full-bridge secondary.

IX. COMPARISON OF THE REVIEWED TOPOLOGIES

The four converter families reviewed in the previous sections approach the 800 VDC to 48 VDC conversion problem from different directions, and each imposes a different balance among switch stress, component count, magnetic complexity, and control effort. These families and their reported variants are summarized in Fig. 24, which classifies each family by the structural or the control choice that distinguishes its members. To have a fair comparison, Table 6 compares the symmetric half-bridge, the full-bridge, the three-level half-bridge under in-phase control, and the three-phase LLC resonant converter with Y-primary and Y-secondary connections. All four are assumed to operate in DCX mode and to deliver the same output power at the same input and output voltages, so

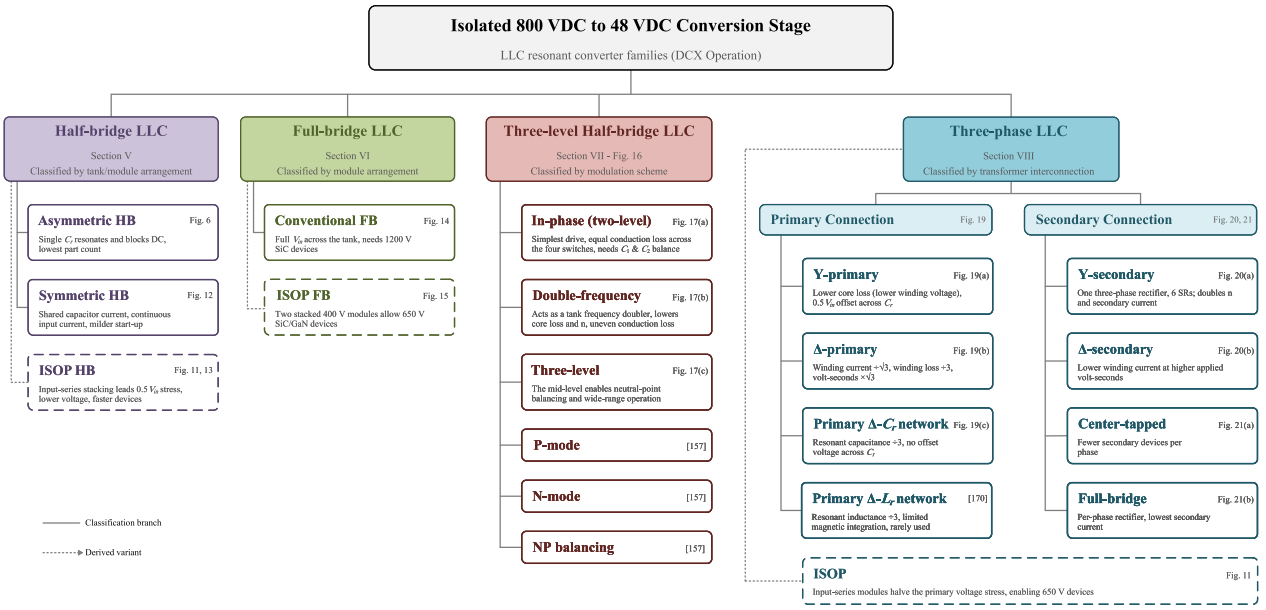


FIGURE 24. Classification of the LLC resonant converter families reviewed for the 800 VDC to 48 VDC conversion stage.

TABLE 6. Comparison of the reviewed LLC resonant converter topologies for the 800 VDC to 48 VDC stage.

Features	Symmetric Half-bridge	Full-bridge	Three-level HB (in-phase control)	Three-phase (Y-primary, Y-secondary)
Number of primary switches	2	4	4	6
Primary switch voltage stress	V_{in}	V_{in}	$0.5V_{in}$	V_{in}
Primary switch rms current	1 (reference)	1/2	1	1/3
Total primary conduction loss	1 (reference)	1/2	2	1/3
Turns ratio (800 V to 50 V)	8:1	16:1	8:1	16:1 per phase
Number of secondary switches	4	4	4	6
Number of transformers (power per trans.)	1 (full power)	1 (full power)	1 (full power)	3 (1/3 each); mergeable into one core by 120-degree flux cancellation
Leakage-based L_r integration	Single tank; L_r realized as leakage without a matching constraint	Same as half-bridge	Same as half-bridge	Three leakages must match for current sharing
Transformer primary voltage; volt-sec. per cycle	$\pm 0.5V_{in}$ square wave; 1 (reference)	$\pm V_{in}$ square wave; 2	$\pm 0.5V_{in}$ square wave; 1	$0.5V_{in}$ per phase; 1 per phase
Output ripple frequency	$2f_s$	$2f_s$	$2f_s$	$6f_s$
Control and modulation	Simple, fixed 50% duty cycle	Simple, fixed 50% duty cycle	Capacitor voltage balancing required	Current sharing depends on tank matching
Main advantage	Lowest part count, reduced capacitor current stress, continuous input current	Halved primary current, full utilization of the input voltage	Halved switch voltage stress enables lower-voltage, faster devices	Lowest per-switch and per-tank current, six-times output ripple frequency
Main limitation	Highest per-switch current	Largest turns ratio	Two devices conduct in series, capacitor voltage balancing	Highest component count, sensitivity to parameter mismatch, complex magnetics
Best-suited domain	Modular building block at moderate power	Extension of mature 400 VDC designs to 800 VDC through ISOP stacking	Operation at megahertz frequency and high power density	High power (above approximately 10 kW) and high output current

that the comparison reflects the topology itself. The same comparison is summarized graphically in Fig. 25, in which the four topologies are rated on five criteria that capture the main tradeoffs, namely switch voltage stress, switch

TABLE 7. Summary of the reviewed converters.

Ref.	V_{in}/V_{out} (V)	Pow. (kW)	f_s (kHz)	Topology	Peak eff. (%)	Pow. den. (W/in³)	Magnetic structure	Key contribution and features
[21]	800/50	20	300	Three-phase LLC with full-bridge secondaries	N/A	129	Tank given as $L_r = 6$ µH, $L_m = 60$ µH, $C_r = 47$ nF and $L_n = 10$	The cascade primary reduces the primary and transformer current
[68]	800/48	12	650	ISOP symmetric half-bridge LLC	98	N/A	Planar matrix transformer with a two-limb structure	The equal air gap across the whole core spreads flux and fully utilizes the core
[69]	800/50	10	1000	Three-level half-bridge LLC	98	N/A	Planar matrix transformer, using multiple outputs to limit secondary conduction loss	The three-level primary halves the device voltage stress, so 650 V GaN is used
[81]	400/48	3	300	Asymmetric half-bridge LLC	98.8	600	Matrix of four elemental transformers and a resonant inductor on a single core	Resonant matrix inductor reduces stacked PCB layers and AC loss; Power density limited by the discrete inductor structure
[82]	400/48	3	250	Asymmetric half-bridge LLC	98.8	600	Matrix of four elemental transformers and four inductors on a six-layer PCB and a single core	Low profile structure
[83]	800/50	6	615	ISOP asymmetric half-bridge LLC	98.75	2070	Two EI transformers merged into a single four-leg core; L_r realized as the leakage inductance of each transformer	Top-side mounting supports liquid cooling; Two matched resonant tanks required; The stacked architecture adds design complexity
[84]	400/48	3	300	Asymmetric half-bridge LLC	98.7	> 1000	Magnetic shunt layer method; The shield layers create a controlled leakage flux used as L_r	Leakage inductance sensitive to shielding layer geometry and manufacturing tolerance
[85]	400/48	3	300	Asymmetric half-bridge LLC	98.7	1500	Two elemental transformers in an EEI core; Unbalanced turns distribution method	Coupled optimization of L_m, L_r and core loss increases design complexity
[127]	400/50	9	330	Asymmetric half-bridge LLC	98.7	1300	Two elemental transformers; Vertically mounted module	Selective SR phase-shifting decouples the hold-up gain from L_m, giving reduction in bulk capacitance against frequency control
[128]	400/50	3.3	N/A	Symmetric half-bridge LLC	98.5	N/A	Series and parallel inductors wound separately but co-assembled with the transformer	Leakage-based integration explicitly rejected as compromising efficiency
[129]	400/50	3	N/A	Symmetric half-bridge LLC	98.5	N/A	L_m integrated into the main transformer structure; L_r as a discrete inductor	States that realizing L_r from transformer leakage constrains the design and compromises converter performance
[136], [137]	800/50	12	1000	ISOP symmetric half-bridge LLC	98.5	> 2500	Leakage inductance of the matrix transformer used directly as L_r	Each module uses a UI core carrying two elemental transformers with two zero-air-gap side legs that share flux
[138]	800/50	11	N/A	ISOP symmetric half-bridge LLC	N/A	1000	Transformers of N ISOP modules merged into one core	Transformer integration technique scales power density with N without increasing core volume
[144]	400/50	8	N/A	Full-bridge LLC	98.7	N/A	Series and parallel resonant inductors built into the transformer cores rather than taken from leakage	The series inductor is placed between the two transformers so the impedance is symmetric as seen by the primary bridges
[145], [146]	400/48	3	1000	Full-bridge LLC	97.3	550	Five-leg core integrating a matrix of four elemental transformers and the resonant inductor	Controllable leakage within the matrix-transformer footprint
[148] – [150]	400/48	3	1000	Full-bridge LLC	98	700	Matrix of two elemental transformers integrated in one elongated UI core; Discrete resonant inductor	The design method requires FEA with measured complex permittivity and conductivity
[159]	800/48	1	700	Three-level half-bridge LLC	96.5	N/A	$L_m = 60$ µH; $L_r = 200$ nH realized as primary leakage inductance; No discrete resonant inductor	Eight paralleled Si SRs add parasitic capacitance that rings the secondary current during dead time
[160]	800/48	3	700	Three-level half-bridge LLC	98.5	650	Matrix transformer with windings added to the side legs of a regular E-core with uniform air gap; Discrete split resonant inductor	Achieves flux shunting through side leg windings, so an off-the-shelf E-core with uniform gap can be used
[163]	400/48	3	1000	Three-phase LLC with Δ-C_r pri. and Y-sec.	97.4	450	Stacked-core method; Dedicated inductor legs stacked vertically on the transformer legs	Stacking the inductor on the transformer cuts core loss by 30 %
[168]	400/48	6	500	Three-phase LLC with Δ-pri. Δ-sec.	99.1	1000	Unbalanced turns distribution method	Realizes all six resonant inductances inside the transformer windings
[171]	400/48	3	1000	Three-phase LLC with Δ-C_r pri. and full-bridge sec.	97.7	600	Three transformers and three inductors in one core; Stacked-core method in planar form	The full-bridge secondary cancels CM noise at its two switching nodes without additional shielding

current stress, structural simplicity, control simplicity, and magnetic simplicity. The ratings in Fig. 25 are qualitative and are derived from the corresponding rows of Table 6: switch voltage stress from the primary switch voltage stress, switch current stress from the primary switch rms current, structural simplicity from the primary and secondary device

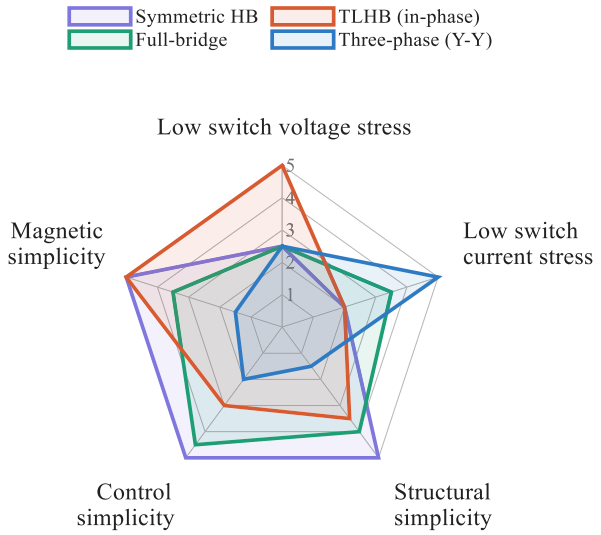


FIGURE 25. Comparison of the four reviewed LLC resonant converter topologies on different criteria.

counts, control simplicity from the control and modulation requirements, and magnetic simplicity from the number of transformers and the leakage-based L_r integration rows. A higher rating denotes a more favorable characteristic under the identical operating conditions assumed in Table 6, and the ratings are intended for relative comparison among the four families rather than as absolute performance measures.

Among the single-phase families, the primary bridge determines both the switch voltage stress and the required transformer turns ratio, and these two quantities cannot be improved simultaneously. The symmetric half-bridge uses only two primary switches and therefore has the lowest part count, but each switch blocks the full input voltage and carries the highest rms current of the four topologies. The full-bridge doubles the voltage applied to the resonant tank, so that the turns ratio doubles and the per-switch rms current is halved. The penalty is four switches that still block the full input voltage, which at 800 VDC requires 1200 V devices. The three-level half-bridge instead retains the half-bridge tank excitation and stacks the four switches so that each blocks approximately half of the input voltage. It is the only topology of the four in which the switch voltage stress is reduced, and this is what permits 650 V GaN devices and megahertz switching on an 800 VDC bus. The cost is that two devices conduct in series, which doubles the total primary conduction loss at equal on-resistance, and that the input capacitor voltages must be kept balanced.

The three-phase converter differs from the single-phase families in kind rather than in degree, because the output power is processed by three interleaved phases instead of one. Two consequences make this attractive for high-power-density designs. First, each phase and its resonant tank process only one third of the total power, so the rms current of each primary switch, and of the resonant inductor and capacitor, is reduced to approximately one third of the half-bridge value at the same input voltage and output power. This directly relaxes the conduction-loss and thermal constraints that dominate the 800 VDC to 48 VDC stage and reduces the need for paralleled primary devices. Second, the magnetic material is used more effectively. This is because the power is distributed over three smaller transformers, which lowers the current per winding and spreads the loss over a larger surface area. In addition, because the fluxes of the three phases are balanced and mutually shifted by 120 degrees, the three transformers can be integrated into a single core, reducing the total core volume. This 120-degree interleaving also raises the output ripple frequency to six times the switching frequency, which lowers the required output filter capacitance. These benefits are obtained at the cost of three resonant tanks, three transformers, and six primary switches, so component count, sensitivity to parameter mismatch, and manufacturing complexity all increase. For this reason, the three-phase topology is generally preferred above approximately 10 kW, where current stress becomes the limiting constraint, whereas the single-phase families remain more attractive at lower power, where their simplicity dominates. Table 7 summarizes the important individual converter designs reported in this literature.

X. CONCLUSION

This paper reviews the emerging 800 VDC power delivery architecture for future AI data centers and the isolated DC–DC converter solutions required for the 800 VDC to 48 VDC stage. The reviewed literature indicates that the transition from conventional 48 VDC rack distribution toward 800 VDC is being driven by the rapid increase in rack power and by the growing limitations of low-voltage distribution in efficiency, current handling, and cabling. In this context, 800 VDC has been presented as a promising approach for improving scalability and enabling higher rack power density in next-generation AI data centers.

The LLC resonant converter operating in DCX mode was reviewed as the basis for this stage, since operating open-loop at the resonant frequency gives a load-independent unity gain and leaves regulation to the downstream stages. The magnetic design of this stage was also reviewed, since the transformer and the resonant inductor account for a large share of the converter loss and volume. Five methods for realizing the resonant inductance as transformer leakage inductance were compared, and the choice among them for this stage is governed by winding loss, profile, and compatibility with the planar matrix structure.

Several converter topologies have been proposed for the 800 VDC to 48 VDC PSU stage. Among the reviewed converter families, each topology offers a different balance among power handling, switch voltage stress, and magnetic complexity. The half-bridge LLC families remain important because they build on a strong data center PSU foundation for 400 VDC to 48 VDC converter stages and offer practical paths toward 800 VDC implementation, although they rely on careful modular arrangements. The full-bridge LLC family also remains important because it provides a

practical building-block approach for extending established 400 VDC to 48 VDC designs to 800 VDC systems. The three-level half-bridge LLC resonant converter is attractive because its reduced primary-side switch voltage stress supports high-frequency operation with lower-voltage devices, but capacitor-voltage balancing and the limitations of each modulation method remain important challenges. The three-phase LLC resonant converter is suitable for higher power levels and reduced output ripple, but it requires more devices and more complex magnetic design. Overall, the literature suggests that future progress will depend on converter solutions that can achieve high efficiency and power density while addressing high secondary-side current, magnetic integration, thermal management, and system-level implementation constraints.

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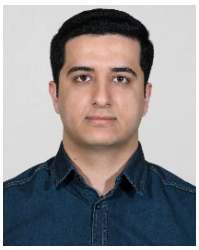
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