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State-of-the-Art Power Electronics in AI Data Centers

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ABSTRACT The rapid scaling of artificial intelligence (AI) workloads is driving a fundamental redesign of the data center power-delivery chain, from the utility grid to the processor die. This review paper presents a stage-by-stage technical benchmarking of state-of-the-art power electronics across the four key conversion stages that define this chain: the power supply unit (PSU), the high-voltage intermediate bus converter (HV IBC), the on-board low-voltage intermediate bus converter (LV IBC) and voltage regulator module (VRM), and the wide-bandgap (WBG) semiconductor devices that enable each stage. For the conventional AC-distributed architecture, totem-pole power factor correction (PFC) and LLC resonant converter topologies are benchmarked across the 3–12 kW power range. The analysis identifies the component-scaling limitations that constrain PSU power density and motivate the transition toward high-voltage direct-current (HVDC) distribution. For the emerging 800 V HVDC architecture, input-series-output-parallel (ISOP)-based GaN LLC converters are shown to achieve power densities exceeding 20 times those of conventional PSUs while maintaining comparable efficiency. In addition, fault-protection challenges unique to DC distribution are systematically analyzed. At the board level, LV IBC, VRM, and direct 48 V-to-point-of-load (PoL) conversion architectures are comparatively evaluated in terms of efficiency, power density, transient response, and thermal performance. This evaluation establishes a topology-to-performance mapping and provides a structured comparison between conventional two-stage and emerging single-stage power-delivery architectures. At the device level, commercial 1200 V SiC MOSFETs are benchmarked against 650 V GaN HEMTs for HVDC applications, while low-voltage Si MOSFETs are compared with 15–100 V GaN HEMTs for board-level conversion stages. Key figures of merit, including Ron×Qg, package area, current density, and cost per ampere, are used to quantify where wide-bandgap technologies have surpassed silicon and where challenges related to cost, current capability, and packaging maturity continue to limit adoption. By consolidating circuit-level and device-level benchmarks within a unified grid-to-chip framework, this review identifies the dominant efficiency–power density–voltage–cost tradeoffs across each conversion stage and provides insights into the development of a scalable, high-density power-delivery ecosystem for next-generation AI server racks .

INDEX TERMS AI data center, grid-to-chip, power supply unit, high-voltage direct current, intermediate bus converter, voltage regulation module, point-of-load, Si MOSFET, GaN HEMT, SiC MOSFET, power density.

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NOMENCLATURE

SST	Solid-State Transformer.
VPD	Vertical Power Delivery.
HVDC	High-Voltage Direct Current.
LVDC	Low-Voltage Direct Current.
PSU	Power Supply Unit.
HV IBC	High-Voltage Intermediate Bus Converter.
LV IBC	Low-Voltage Intermediate Bus Converter.
VRM	Voltage Regulator Module.
PoL	Point-of-Load.
PFC	Power Factor Correction.
LLC	Inductor–Inductor–Capacitor.
HB	Half-Bridge.
FB	Full Bridge.
IS-HB	Input-Series Half-Bridge.
ISOP	Input-Series Output-Parallel.
3Φ-IL TP	Three-Phase Interleaved Totem-Pole.
3Φ-IL FB	Three-Phase Interleaved Full-Bridge.
IL TP	Interleaved Totem-Pole.
SC	Switched Capacitor.
DP Series-Cap	Dual Path Series-Capacitor.
TP Series-Cap	Tri-Path Series-Capacitor.
SS-SC	Series-Stacked Switched Capacitor.
ReSC	Resonant Switched-Capacitor.
ZIV	Zero Inductor Voltage Converter.
SHC	Symmetric hybrid converter.
ReSC-PL	ReSC- Parallel Inductor.
CCP	Charge Converging Phase.
MDHC	Modified Dickson Charge-Pump Hybrid Buck.
IP-TLVR	Inverted-Pyramid Trans-Inductor Voltage Regulator.
SC-MO	Switched Capacitor with Multiple Output.
M-Φ DPC	Multi-Phase Direct Power Converter.
XQSD	Cross-Coupled Series-Capacitor Quadruple Buck.
DP-MIH	Dual-Phase Multi-Inductor Hybrid.
SDIH	Symmetric Dual Inductor Hybrid.
3L-HB CD	3-Level Half-Bridge with Current-Doubler.
ACF	Active-Clamp Forward.
Sigma	LLC DCX in series with Buck.
Hybrid ReC	Hybrid Resonant Converter.
FB-HT CD	Full-Bridge Half-Turn Transformer with CD.
SCB	Series-Capacitor-Buck.
Dickson^2	Dickson-Squared Hybrid SC.
LEGO	Ladder-based Hybrid Point-of-Load Converter.
VIB	Virtual Intermediate Bus.
CaSP	Cascaded Series-Parallel.
CP	Charge Pump.
BCD	Bipolar-CMOS-DMOS.
DCX	DC Matrix Transformer.
M-Φ DCX	Multi-Phase DC Transformer.
CCM	Continuous Conduction Mode.
DCM	Discontinuous Conduction Mode.
CrCM	Critical Conduction Mode.
TCM	Triangular Conduction Mode.
ZVS	Zero-Voltage Switching.
ZCS	Zero-Current Switching.
Lr	Resonant Inductance.
Cr	Resonant Capacitance.
Lm	Magnetizing Inductance.
LGA	Land Grid Array.
TLVR	Trans-Inductor Voltage Regulator.
Pk Eff.	Peak Efficiency.
FL Eff.	Full-Load Efficiency.

I. INTRODUCTION

Data centers, which originated in the 1960s as centralized "computer rooms" for single mainframes, have evolved into vast, highly interconnected infrastructures that now power global digital services. This evolution has brought immense energy demand, with data centers already accounting for a significant share of worldwide electricity consumption [1], [2]. In 2024, as per a report, they have consumed around 415 TWh, which accounts for about 1.5% of global electricity and is expected to exceed 945 TWh by 2030 [3], roughly equivalent to Japan's current annual consumption. The majority of this energy consumption, i.e., 50%, is consumed by cooling systems properly dissipating the heat from the data centers, followed by servers and storage at 26%, power conversion at 11%, network hardware at 10%, and lighting at 3%. The rapid adoption of artificial intelligence (AI) has been a major driver of this trend, as AI workloads demand advanced hardware, high-speed data processing, and large-scale computing and storage resources to sustain compute-intensive operations and fuel digital innovation [4]. The scale of these demands is highlighted by the exponential growth in compute power, which has been doubling approximately every 3.4 months. This growth parallels the surge of the global AI market, projected to reach $1811.8 billion by the end of 2030 [5]. Consequently, AI data center capacity is expected to expand at an average annual rate of 33% through 2030, far outpacing historical growth [6].

Each new generation of AI graphical processing unit (GPU) increases compute performance and power demand. For example, Nvidia's server series A100 and H100 consume 400 W and 700 W, respectively, and the upcoming Blackwell B200 may draw up to 1200 W per GPU, with dual B200 + Grace CPU configurations reaching 2700 W [7]. At the server level, an NVIDIA DGX H100 with 8 GPUs consumes around 10200 W. At the rack level, AI data centers now operate at 30–100+ kW per rack, far above traditional 7–10 kW racks [8]. This rapid growth in GPU and server power has driven data center electricity demand to unprecedented levels [2], [9], highlighting the urgent need for efficient power delivery and conversion from the utility grid to the chip.

Currently, the AC power distribution for data center infrastructure, as shown in Fig. 1, delivers 85–305 VAC to each rack through a power distribution unit (PDU). Within the rack, the AC input is first converted to 50 VDC by a

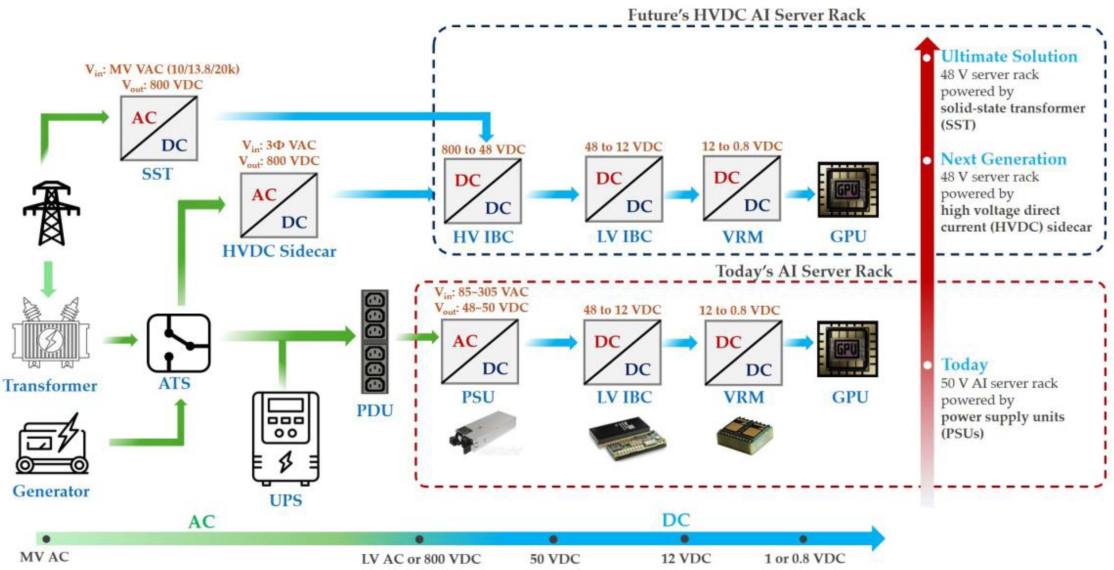


FIGURE 1. Grid-to-chip power delivery solutions for AI data centers, highlighting current LV AC distribution architecture and emerging HVDC distribution architecture to meet escalating power demands.

power supply unit (PSU). This 50 VDC is then stepped down to 12 VDC using an low-voltage intermediate bus converter (LV IBC) and finally regulated to 1 to 0.8 VDC by a voltage regulator module (VRM) for direct power delivery to the AI GPU [10]. In this AC distribution scheme, each AI server rack houses six 3–5.5 kW PSUs on a single shelf, delivering up to 33 kW per shelf. With multiple shelves installed, the total rack power can exceed 100 kW [11]. However, in a typical AI rack, most of the space is allocated to compute, storage, and networking, leaving limited room for additional power shelves or battery backup units. This spatial constraint, combined with the growing power demands of next-generation AI workloads, highlights the urgent need for more compact and efficient power conversion solutions.

The next-generation high-voltage direct current (HVDC) power distribution architecture addresses these challenges by streamlining the conversion path [12], as shown in Fig. 1. In this scheme, an HVDC sidecar converter converts 3-phase 400–480 VAC into 800 VDC, which is then distributed to each rack. In future implementations, solid-state transformers (SSTs) are expected to interface directly with the medium-voltage utility grid, providing a more compact and efficient conversion to 800 VDC. Within each rack, this HVDC input is stepped down to 50 VDC by an isolated high-voltage intermediate bus converter (HV IBC), which supplies LV IBCs and downstream point-of-load VRMs on each server tray [13]. HVDC distribution can be implemented at multiple levels. At the rack level, isolated HV IBCs can supply up to 90 kW per shelf, supporting high-power operation without excessive PSU overhead [14]. At the tray level, high-power-density power distribution boards (PDBs) equipped with multiple parallel HV IBC modules can achieve power densities of up to 500 W/in^3, ensuring high-efficiency and high-density power delivery down to the chip level. Compared with conventional AC distribution, this HVDC architecture improves efficiency, reduces copper usage, and frees valuable rack space for compute function.

The on-board conversion stages present particularly demanding challenges as AI processor currents scale toward the kilo-ampere regime. In the conventional two-stage architecture, an LV IBC performs bulk voltage conversion from the 50 VDC rack bus to a 12 VDC intermediate rail, followed by a VRM that provides final point-of-load (PoL) regulation at 0.7–1.8 VDC [15], [16]. As AI accelerator power continues to increase, the Blackwell B200 GPU, for example, can draw up to 1.2 kW at peak load, corresponding to a theoretical current of approximately 1200 A at 1 V. Under these conditions, losses associated with the IBC and power distribution network (PDN) become increasingly significant. Consequently, growing attention has been directed toward single-stage direct-conversion architectures, which convert the 50 VDC rack bus directly to the processor supply voltage and eliminate the intermediate 12 V rail [17].

The primary objective of this review is to consolidate industrial and academic benchmarking data within a unified grid-to-chip framework, enabling direct comparison of efficiency, power density, transient performance, and semiconductor characteristics across the power-delivery chain. Specifically, this review identifies the key efficiency–power density tradeoffs and topology evolution at each conversion stage, evaluates the advantages of wide-bandgap devices over silicon in both high-voltage and low-voltage applications, and highlights technology pathways toward scalable, high-density power delivery for next-generation AI data centers.

Accordingly, this review benchmarks state-of-the-art power-conversion topologies and semiconductor devices used

TABLE 1. Key Specifications of PSU From Industrial Institutes

Reference	Power [kW]	Pk Eff. [%]	FP Eff. [%]	Volume [mm] L x W x H	Cooling system	EMI Filter	@Vin [V_{AC}]
STM [21]	3	96.3	96	105 x 281 x 41	Fans Included	Included	230
Infineon [22]	3	97.47	96.26	520 x 73.5 x 40	Fan included	Included	230
Infineon [23]	3.3	97.2	96.6	192 x 72 x 40	Fan included	Included	230
TI [24]	3.6	96	~	185 × 73.5 × 40	Fan included	Included	230
Navitas [25]	4.5	97.2	96.6	~	Fan included	~	230
Infineon [26]	8	97.5	96.5	450 x 73.5 x 40	Fan included	Included	230
TI [27]	8	97.5	~	700 x 68 x 32	~	~	~
Navitas [28]	8.5	98	~	560 x 73.5 x 40	Fan included	Included	~
Infineon [29, 30]	12	97.75	96.6	640 x 68 x 40	Fan included	Included	230
Navitas [31]	12	97.5	96.5	790 x 73.5 x 40	Fan included	Included	277
Onsemi [32]	12	98	~	750 x 80 x 42	Fan included	~	277

in AI server power delivery. Section II examines PSU designs in the 3–12 kW range, covering TP-PFC and LLC stages. Section III evaluates HV IBC topologies from 1–20 kW, including input-series half bridge (IS-HB), HB and full bridge (FB) LLC, and input-series output parallel (ISOP) architectures. Section IV analyzes on-board power conversion, including LV IBCs, VRMs, and direct 48 V-to-PoL converters, together with a comparison of two-stage and single-stage architectures. Section V presents a device-level benchmarking of commercial SiC MOSFETs, GaN HEMTs, and silicon devices using Ron×Qg, package area, current density, and cost. Finally, Section VI summarizes the key tradeoffs across the power-delivery chain and outlines future technology directions. Collectively, this review serves as a unified reference for power electronics designers and system architects developing next-generation AI data center power-delivery systems.

II. POWER SUPPLY UNIT (PSU)

Rising rack power demands from AI workloads have pushed traditional 12-VDC distribution to its limits, where increased copper losses and bulky conductors constrain both efficiency and power density [18], [19]. To overcome these limitations, the open compute project (OCP) standardized a 50-VDC distribution infrastructure, reducing distribution losses by more than 30%. Within this architecture, PSUs convert AC input to regulated 50 VDC distribution and support multi-kW scalability. A typical PSU consists of two main conversion stages: a front-end AC–DC power factor correction (PFC) stage and a back-end isolated DC–DC LLC converter for output voltage regulation. In addition, PSUs integrate electromagnetic interference (EMI) filters, as well as cooling and monitoring systems that enable load balancing among units to mitigate thermal hotspots. According to Yole Group, the AI data center PSU market is projected to exceed $14 billion by 2030, driven primarily by high-power applications. To improve energy efficiency, the industry follows the 80 PLUS certification standard, which ranges from Basic to the recently introduced Ruby tier. Notably, the Titanium tier requires efficiencies of 90% at 10% load, 96% at 50% load, and 91% at full load (FL) (230 V input), driving the adoption of highly efficient PSU designs [20].

Table 1 summarizes industry-reported PSU's for AI data centers operating at a 50 VDC output. As the output power scales from 3 kW to 12 kW, the peak (Pk) efficiency consistently remains within ∼96%–98%, while the FL efficiency varies only slightly (∼96%–96.6%). This trend highlights the strong scalability and optimized design of modern PSU's. Most efficiency data are measured at an input voltage of 230 VAC; however, the 12 kW PSUs from Navitas Semiconductor and Onsemi are characterized at 277 VAC. Fig. 2 illustrates the relationship between power density (W/in^3) and power rating (kW). Despite maintaining high efficiency across increasing power levels, the power density of PSUs generally decreases as output power rises. This reduction is driven by several design trade-offs. Higher power levels require interleaved topologies, increasing device count (from 10 at 3 kW to 133 at 12 kW) and necessitating larger heat sinks and cooling systems. Stricter EMI requirements add bulkier filter networks, while transformers and other passive components must scale to handle higher currents. Together, these factors increase system volume and reduce overall power density. In contrast to this general trend, Infineon has demonstrated a 12 kW PSU achieving a remarkable power density of 113 W/in^3. This improvement is driven by advanced architecture such as a 2× interleaved 3-level flying capacitor PFC, power pulsation buffering, and an ISOP LLC converter, which enhance power handling while reducing volume. Fig. 3 shows a circuit schematic of a PSU consisting of a 3-phase interleaved totem-pole (3-Φ IL TP) PFC front-end and a FB LLC resonant DC–DC stage, delivering a regulated 50 VDC output.

A. POWER FACTOR CORRECTION (PFC)

The PFC stage plays a critical role in modern high-power PSUs by ensuring efficient AC–DC conversion with minimal

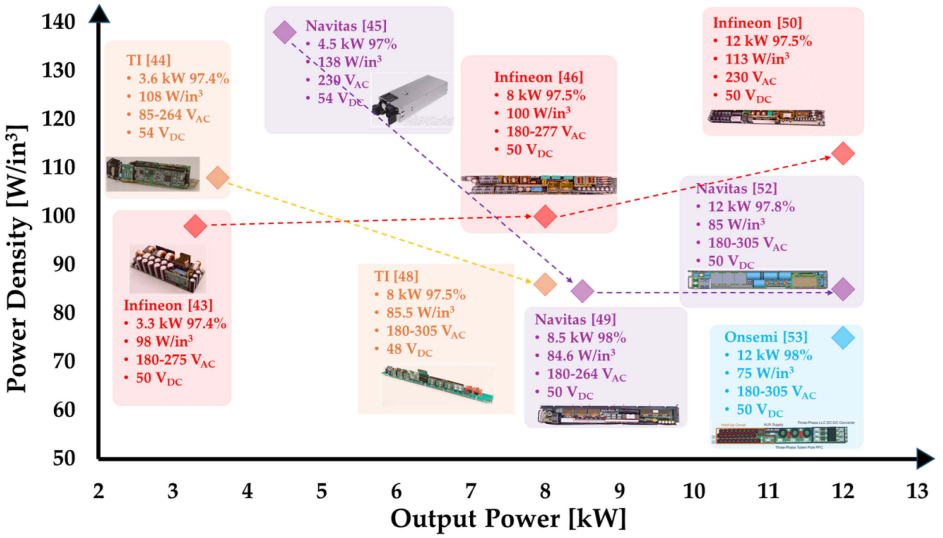


FIGURE 2. Power density (W/in³) versus power rating (kW) for representative power supply unit's (PSU's) in AI data centers.

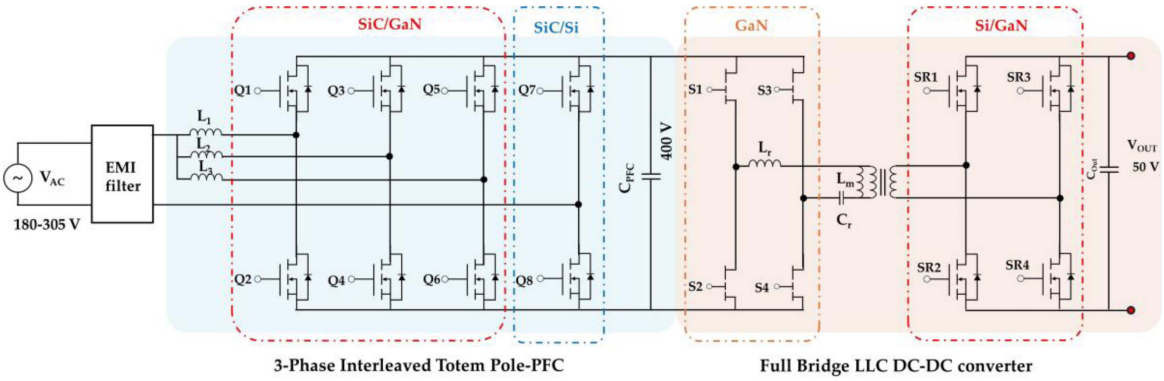


FIGURE 3. Circuit topology of a two-stage isolated power supply unit (PSU), featuring a 3-Phase interleaved totem-pole (3-Φ ILTP) power factor correction (PFC) stage, followed by a full bridge (FB) LLC resonant DC–DC converter stage, designed to deliver a regulated 50 VDC output.

losses and near-unity power factor [33], [34]. Table 2 provides a comprehensive overview of the PFC stage in PSUs, including efficiency, switching frequency, topology, control strategies, and the semiconductor technologies employed. The TP PFC topology has emerged as the dominant solution due to its ability to replace the conventional diode bridge with actively controlled switches, thereby reducing conduction losses and improving overall efficiency. From an operational perspective, the TP PFC conducts during both positive and negative half-cycles of the AC input. One leg operates at high frequency while the other switches at low frequency, enabling effective current shaping. The boost inductor current is controlled to follow the input voltage waveform, ensuring a near-unity power factor. In practice, continuous conduction mode (CCM) dominates across most PSU designs due to its lower current ripple, reduced peak current stress, and simpler EMI filtering, making it well suited for high-power applications. However, CCM operation introduces higher switching losses at elevated frequencies [35]. To address this, alternative modes such as triangular conduction mode (TCM) are explored in specific designs [36]. For example, the TI 8 kW GaN-based TP PFC adopts TCM to achieve soft switching and enable higher switching frequencies (70 kHz–1.2 MHz). While this reduces switching losses, it comes at the cost of higher peak and root mean square (RMS) currents, increased conduction losses, and greater control complexity, which limits its adoption in high-power systems.

As PSU power levels increase, the PFC architecture evolves to accommodate higher current and power demands. At lower power levels (up to ∼3.6 kW), single-Φ TP PFC operating in CCM is typically sufficient. As the power scales to around 8 kW, IL TP configurations are adopted, where phase-shifted parallel stages share current across phases, reducing the effective input and output capacitor ripple, and spreading power dissipation across multiple switching devices and magnetic components to mitigate localized thermal hotspots.

TABLE 2. Key Specifications of PFC Stage in PSU From Industrial Institutes

Ref	Power [kW]	Vin AC	Pk Eff. [%]	FP Eff. [%]	PF	iTHD [%]	Freq [kHz]	Topology	Control	HF/LF Semi
STM	3	90-264	98.6	98.5	0.98	5	70	TP	CCM	650 V SiC 650 V Si
Infineon	3	180-275	99	98.7	0.99	2	65	TP	CCM	650 V SiC 650 V Si
Infineon	3.3	180-275	98.9	98.8	0.98	5	65	IL TP	CCM	650 V SiC 600 V Si
TI	3.6	90-265	98.93	98.5	>0.99	<2	65	TP	CCM	650 V GaN
Navitas	4.5	230	~	~	~	~	75	IL TP	CCM	650 V SiC 650 V Si
Infineon	8	180-277	99.07	98.8	>0.995	3.5	65	IL TP	CCM	650 V SiC 650 V SiC
TI	8	180-305	~	~	~	~	70-1200	3Φ-ILTP	TCM	650 V GaN
Navitas	8.5	180-264	~	~	~	~	~	3Φ-IL TP	CCM	SiC/Si
Infineon	12	180-305	99.35	98.81	0.995	3.5	32.5	3-level flying cap IL TP	CCM	400 V SiC 600 V SiC
Navitas	12	180-305	~	~	~	~	50	3Φ-IL TP	hybrid CCM/CrCM	650 V SiC 650 V Si
Onsemi	12	180-305	~	~	~	5	~	3Φ-IL TP	~	750 V SiC 750 V SiC

At higher power levels (∼12 kW), 3-Φ ILTP architectures extend these same benefits, ripple cancellation, EMI suppression, and thermal distribution further across three phases. In advanced implementations, such as the 12 kW PSU developed by Infineon, the TP-PFC stage is further enhanced through a 3-Φ interleaved, 3-level flying-capacitor topology. In this topology, the flying-capacitor bridge leg functions as the high-frequency switching network, where controlled insertion of the flying capacitor generates multiple voltage levels across the boost inductor [29], [37]. The resulting reduction in voltage stress, switching losses, and inductor current ripple enables operation at higher switching frequencies while maintaining high conversion efficiency. Consequently, the required inductance is reduced, allowing the use of low-profile magnetic components that satisfy stringent 1/2U server form-factor constraints [38].

Across the entire power range, the PFC stage maintains consistently high efficiency, with Pk efficiency slightly improving as output power increases reaching up to 99.35% at 12 kW primarily due to better utilization of semiconductor devices and the reduced relative impact of fixed losses at higher power levels. Despite the added complexity from interleaving and multi-phase operation, advanced topologies such as ILTP and 3Φ-ILTP sustain high FL efficiency (∼98.8–98.81%), demonstrating that modern designs can scale in power without compromising performance. At the same time, power quality remains well controlled, with the power factor staying close to unity (0.98–0.995) and input current total harmonic distortion (iTHD) maintained within ≤5% in most cases, meeting the stringent requirements defined by the OCP v3 specifications across varying load conditions.

B. INDUCTOR-INDUCTOR-CAPACITOR (LLC)

Following the PFC stage, the PSU employs an isolated LLC resonant converter to step down the 400 VDC to an intermediate 50 VDC output. A HB or FB converts the DC input into high-frequency AC, which excites the resonant tank (Lr–Cr–Lm) and drives a high-frequency isolation transformer [39], [40]. The transformer turns ratio provides the primary voltage conversion, while synchronous rectification and output filtering generate the regulated 50 VDC output. Resonant operation enables the primary-side switches to achieve zero-voltage switching (ZVS), while the secondary-side rectifiers operate under near zero-current switching (ZCS), thereby minimizing switching losses, device stress, and electromagnetic interference. These characteristics enable high efficiency and power density, making the LLC converter the dominant DC–DC topology in modern server PSUs. Table 3 summarizes the reported LLC converter implementations, including efficiency, switching frequency, topology, transformer design, and semiconductor technologies.

A clear topological evolution is observed in LLC converters with increasing power. HB configurations dominate at power levels of up to approximately 3.3 kW, owing to their circuit simplicity, reduced component count, and cost-effectiveness. For power levels ranging from 3.6 kW to 8 kW, FB topologies are preferred, as they offer improved DC bus utilization and reduced current stress, though at the expense of a higher component count. At the 8-kW level, TI utilizes a 3-Φ delta–delta (Δ–Δ) connected LLC converter. In this configuration, three phase-shifted inverter legs drive delta-connected transformers. This setup allows for reduced output ripple, enables higher switching frequency operation, enhances magnetic utilization, and lowers RMS currents [41]. However, it also introduces significant design and control complexity [42]. For higher power levels, advanced architectures such as 3Φ LLC, 3-Φ interleaved FB (3-Φ IL FB) LLC, and ISOP configurations are utilized to distribute power processing demands and improve current sharing among converter modules. In a 3-Φ LLC converter with either Y or Δ configuration, the 120° phase-shifted

TABLE 3. Key Specifications of LLC Stage in PSU From Industrial Institutes

Ref	Power [kW]	Vout [DC]	Pk Eff. [%]	FP Eff. [%]	Topology	Transformer	Freq [kHz]	Pri/Sec Semi
STM	3	53.5	98.2	no data	FB	18:5	80-150	650 V Si 80 V Si
Infineon	3	50	98.4	98	HB	16:4	45-250	600 V Si 80 V Si
Infineon	3.3	50	98.45	97.98	HB	8:2	~	650 V GaN 80 V Si
TI	3.6	54	98.68	97.17	FB	~	~	650 V GaN 100 V GaN
Navitas	4.5	54	~	~	FB	~	300	650 V GaN
Infineon	8	50	98.74	98.25	FB	2 x 8:2	380-540	650 V GaN 80 V Si
TI	8	48	~	~	Δ-Δ 3-Φ	~	200-1500	650 V GaN 100 V GaN
Navitas	8.5	54	~	~	3-Φ	~	~	GaN
Infineon	12	50	98.65	98.25	ISOP	2 x 9:2	425	400 V SiC 80 V Si
Navitas	12	54	~	~	3-Φ IL FB	~	120	650 V GaN
Onsemi	12	50	~	~	3-Φ	~	~	750 V SiC

inverter legs establish coupled resonant operation, wherein each phase current is interdependent with all three resonant tanks. During each half-cycle, energy is simultaneously delivered to the load and exchanged among phases, ensuring continuous and uninterrupted power flow [43]. This inherent inter-phase coupling reduces sensitivity to component tolerances and facilitates natural current sharing without the need for additional control intervention. In contrast, the 3-Φ ILFB LLC employs phase-shifted operation across multiple full-bridge modules, where each phase maintains an independent resonant tank with no electrical coupling between phase [44]. Further, ISOP topology connects converter modules in series at the input to distribute voltage stress and in parallel at the output to share current, thereby reducing both device voltage and current stress; however, this arrangement necessitates dedicated control mechanisms for voltage balancing and current sharing [45], [46]. These advanced LLC topologies collectively introduce increased design complexity, elevated semiconductor device count, and higher implementation cost [47].

The LLC stage maintains high Pk and FL efficiency, typically exceeding 97–98.7%, with switching frequencies ranging from 115 kHz to 1.5 MHz. Higher switching frequencies, enabled by soft-switching operation and wide-bandgap (WBG) semiconductor devices, significantly reduce passive component size, thereby enhancing power density. The high-frequency transformer is a key determinant of this density, as its core size and winding volume scale inversely with frequency. However, at elevated power levels, increased current handling requirements introduce higher copper losses, necessitating larger cores, thicker conductors, or multiple transformers for power sharing, ultimately offsetting the benefits of high-frequency operation and limiting power density improvements.

C. PSU SEMICONDUCTOR AND THERMAL ANALYSIS

The high-frequency (HF) leg of a TP-PFC operates under hard-switching conditions, making switching-related parameters such as gate charge (Q_G), output capacitance (C_{oss}), on-state resistance (Ron), and reverse-recovery charge (Q_{rr}) critical [33], [48]. Higher Q_G and C_{oss} increase switching losses, while body-diode reverse recovery significantly penalizes Si devices [49], [50]. Consequently, device selection requires balancing switching and conduction losses through the Ron–Q_G tradeoff. GaN HEMTs offer the lowest charge and negligible reverse recovery [51], [52], enabling higher switching frequencies and power density, whereas SiC MOSFETs provide a balanced combination of low Ron, moderate Q_G, superior thermal capability, and robust hard-switching performance [53]. Therefore, SiC MOSFETs dominate the high-frequency leg of modern server PFC stages, as summarized in Table 2. In contrast, the low-frequency (LF) leg functions as a synchronous rectifier at the line frequency (50/60 Hz), where conduction losses dominate and switching losses are negligible. As a result, ultra-low Ron is the primary device-selection criterion, whereas Q_G is less critical. Consequently, low-Ron Si MOSFETs remain the most widely adopted devices in the LF leg, as shown in Table 2. To further improve power density, some advanced PFC designs incorporate a baby-boost energy buffer between the PFC and LLC stages to mitigate double-line-frequency power pulsations [54], [55]. By reducing DC-bus ripple, the buffer minimizes the required electrolytic capacitance and enables a more compact design. Since high-speed switching is not required, cost-effective 600 V Si devices are typically employed, albeit at the expense of additional circuit complexity. The LLC converter achieves ZVS on the primary side, making both Ron and C_{oss} key device-selection parameters [40]. However, achieving lower Ron typically requires a larger die area

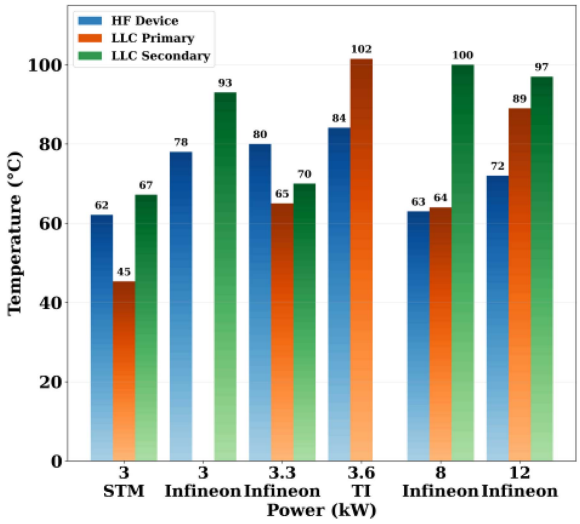


FIGURE 4. Temperatures of the PFC high-frequency leg, LLC primary and LLC secondary switches for reported PSU designs.

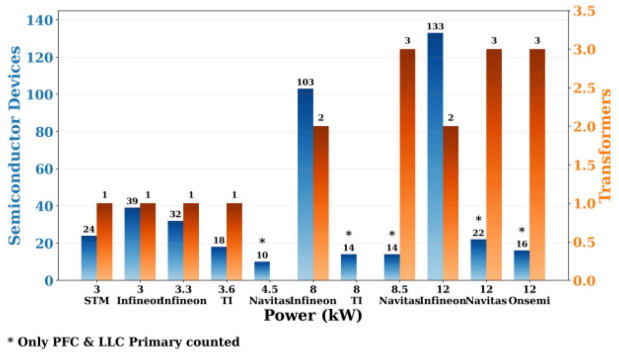


FIGURE 5. Semiconductor device and transformer count for 3–12 kW PSU designs.

and, consequently, higher C_{oss} [50]. While SiC MOSFETs provide very low Ron, their higher C_{oss} increases circulating energy in the resonant tank [56]. In contrast, GaN HEMTs offer a more favorable combination of low Ron and low Coss, making them well suited for high-frequency, high-power-density LLC converters. As a result, GaN HEMTs dominate primary-side implementations. The LLC secondary side operates ZCS, causing conduction losses to dominate. Consequently, low-voltage (80–100 V) devices with ultra-low Ron are preferred to maximize efficiency and current capability. In this voltage range, GaN HEMTs provide lower Ron and support MHz-class operation, enabling higher efficiency and power density than Si MOSFETs, although with additional reliability considerations [51], [52].

Fig. 4 shows the measured temperature distribution of key components in PFC and LLC stages under FL operation (230 VAC). The PFC HF leg consistently exhibits elevated temperatures (≈62–84°C), reflecting significant hard-switching losses and higher switching stress. In contrast, the LLC primary operates at relatively moderate temperatures (≈45–89°C) due to ZVS, which effectively reduces switching losses despite high-frequency operation. The LLC secondary side, however, reaches the highest temperatures (≈67–100°C), confirming that conduction losses dominate in this stage due to the high output current at low voltage. Notably, at higher power levels (8–12 kW), the secondary-side temperatures remain the most critical [57]. Overall, these results indicate that thermal stress transitions from switching-dominated losses in the PFC stage to conduction-dominated losses in the LLC secondary stage, which strongly influences semiconductor selection across different stages of the PSU.

D. NO ROOM IN RACK FOR HIGH POWER DEMAND

The relationship between output power and component count in AI data center PSUs reveals a clear scaling trend in system complexity. As the output power increases from 3 kW to 12 kW, the number of transistors rises significantly, from approximately 18–39 devices at lower power levels to over 100 devices (up to 133) at 12 kW. This increase is primarily driven by the adoption of interleaved and multi-phase topologies, such as interleaved TP PFC and 3-Φ LLC converters, which enable current sharing, reduce losses, and improve thermal performance. In parallel, the number of transformers increases from a single unit at low power to multiple units (2–3 or matrix configurations) at higher power levels to facilitate power distribution and reduce current stress, as illustrated in Fig. 5.

This scaling in semiconductor devices and magnetic components directly leads to increased system volume, cost, and design complexity. This challenge is further intensified by the rapid growth in AI server power demand, which has escalated from tens of kilowatts to beyond 1 MW per rack (e.g., Rubin Ultra). At the same time, rack-level space is severely constrained, with a significant portion already occupied by compute hardware. Consequently, there is limited room for additional power shelves, battery backup units (BBUs), or transient energy storage elements such as supercapacitors. These constraints highlight the critical need for more compact, thermally efficient, and highly integrated power delivery architectures, as conventional PSU scaling is approaching its practical limits.

III. HIGH VOLTAGE INTERMEDIATE BUS CONVERTER (HV IBC)

As established in Section I, conventional PSU-based power distribution becomes impractical beyond 200 kW rack loads, where Kyber-class racks would require nearly 200 kg of copper busbars and devote a significant portion of rack space to power shelves alone. To address these challenges, NVIDIA announced its 800-VDC rack power architecture at the 2025 GTC conference [58]. The solution employs an 800-VDC sidecar that integrates the power shelf, BBUs, and supercapacitors into a single cabinet, capable of powering up to 576 Rubin Ultra GPUs within a Kyber rack. By centralizing AC-to-HVDC conversion and distributing 800 VDC directly throughout the rack, this architecture reduces copper usage,

TABLE 4. Key Specifications of HVDC IBC From Academic Industrial Institutes

Ref	Vin-Vout	Power (kW)	Density (W/in^3)	Pk Eff. [%]	FP Eff. [%]	Freq [kHz]	Volume [mm] L x W x H	Topology	Transformer	Pri/Sec Semi
TI [61]	800-12	1	78.1	98	97.7	~	50 x 120 x 35	IS-HB	~	650 V GaN 40 V Si
Seoul Tech [62]	800-14	1.2	167.2	93	~	700	71 x 156.6 x10.6	IS-HB	2*6:1	600 V GaN
CNU [63]	800-48	1.2	~	96.3	95.8	100	~	IHSTD	2:1	SiC/GaN/Si
NCSU [64]	1000-48	2.5	~	97.2	96	36	~	HB-LLC	10:1	1.7 kV SiC 80 V GaN
Uni. Arkansas [65]	800-48	5	81.9	97.8	97.4	100	142.6 x 75.2 x 89.4	HB-LLC	8:1:1	1.2 kV SiC 150 V Si
Seoul Tech [66]	800-48/12	6	~	96.6	95.9	140	~	FB-LLC	~	1.2 kV SiC 100 V Si
STM [67]	800-12	6	2500	97.5	~	850	~	ISOP	~	700 V GaN 40 V Si
Eaton [68]	1000-48	10	~	98.4	97	27	~	HB-LLC	~	1.7 kV SiC 100 V Si
STM [67]	800-50	12	2600	98	~	~	~	ISOP-LLC	~	650 V GaN 100 V GaN
EPC [69]	800-12.5	6	2514	97	~	1000	104 x 47 x 8	ISOP	8*4:1:1	150 V GaN 40 V GaN
NCSU [70]	1000-48	20	~	97	94	30	~	HB-LLC	~	1.7 kV SiC 100 V Si
Navitas [71]	800-6	20	2100	96.5	~	1000	~	ISOP	Center-tap	650 V GaN 25 V Si
STM [67]	800-6	20	~	96.5	~	650	~	ISOP	~	120 V GaN 25 V Si

frees valuable rack space for compute resources, simplifies the power-delivery chain, improves thermal management, and enhances overall system efficiency [59], [60].

Table 4 summarizes academic and industry reported HVDC IBC implementations for AI data center applications operating with a 50 VDC output. At power levels of 1–1.2 kW, converters can achieve very high efficiency due to reduced conduction losses in semiconductors, transformer windings, PCB interconnections, and thermal management components. For example, the 1 kW TI converter achieved a Pk efficiency of 98% and an FL efficiency of 97.7%. As the power level increases, efficiency remains high but begins to show a slight decline. The 2.5 kW NCSU converter reported a Pk efficiency of 97.2% and a FL efficiency of 96%, while the 5 kW converter achieved a Pk efficiency of 97.8% and an FL efficiency of 97.4%. At higher power levels, Eaton's 10 kW converter achieved a Pk efficiency of 98.4%, although its FL efficiency decreased to 97%, while the 12 kW STM converter reported a Pk efficiency of 98%. These results demonstrate that carefully optimized resonant topologies can maintain high efficiency even at elevated power ratings. The efficiency degradation becomes more pronounced in the 20 kW class. The 20 kW NCSU converter achieved a Pk efficiency of 97%, but its FL efficiency dropped to 94%, representing one of the largest Pk-to-FL efficiency reductions among the reported designs. In comparison, both the 20 kW Navitas ISOP converter (800 V/6 V) and the 20 kW STM ISOP converter (800 V/6 V) achieved Pk efficiencies of 96.5%. As a result, maintaining high efficiency becomes increasingly challenging as power levels rise. The corresponding increase in output current leads to higher conduction losses, greater circulating current in the resonant tank, increased copper and magnetic losses, elevated operating temperatures, and potential current-sharing imbalances among parallel devices or converter modules [72]. Fig. 6 illustrates the relationship between Pk efficiency and power rating for representative HVDC IBCs reported in both academic and industrial literature.

A. HVDC IBC TOPOLOGIES

The HV IBC stage must achieve a high step-down ratio (16:1) while providing galvanic isolation, soft-switching operation, high conversion efficiency, and effective load regulation. To meet these requirements, most reported HV IBC designs employ LLC-based isolated converters that utilize high-frequency transformers. The choice of HVDC IBC topology is primarily determined by power level, voltage stress, output current, and power-density requirements. As power levels increase, converter architectures typically evolve from simple single-cell implementations to modular multi-cell structures, such as ISOP-based LLC converters, to improve scalability, current sharing, and thermal performance.

In low power converters, such as the 1 kW TI and 1.2 kW Soul Tech designs, IS-HB topology adopted and implemented using GaN devices. In this topology, the input voltage is shared between two series-connected modules, such that each primary-side switch is subjected to only half of the total bus voltage [73], as illustrated in Fig. 7(a). This enables the use of 650 V GaN devices on the primary side, leveraging their

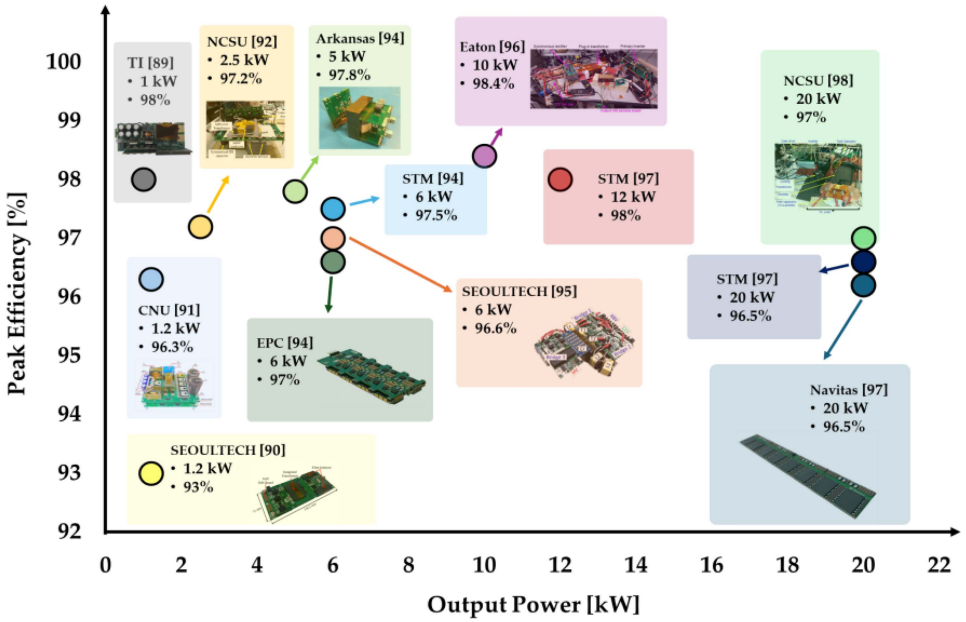


FIGURE 6. Peak efficiency (%) versus power rating (kW) for representative HVDC IBC reported by academic and industrial institutes.

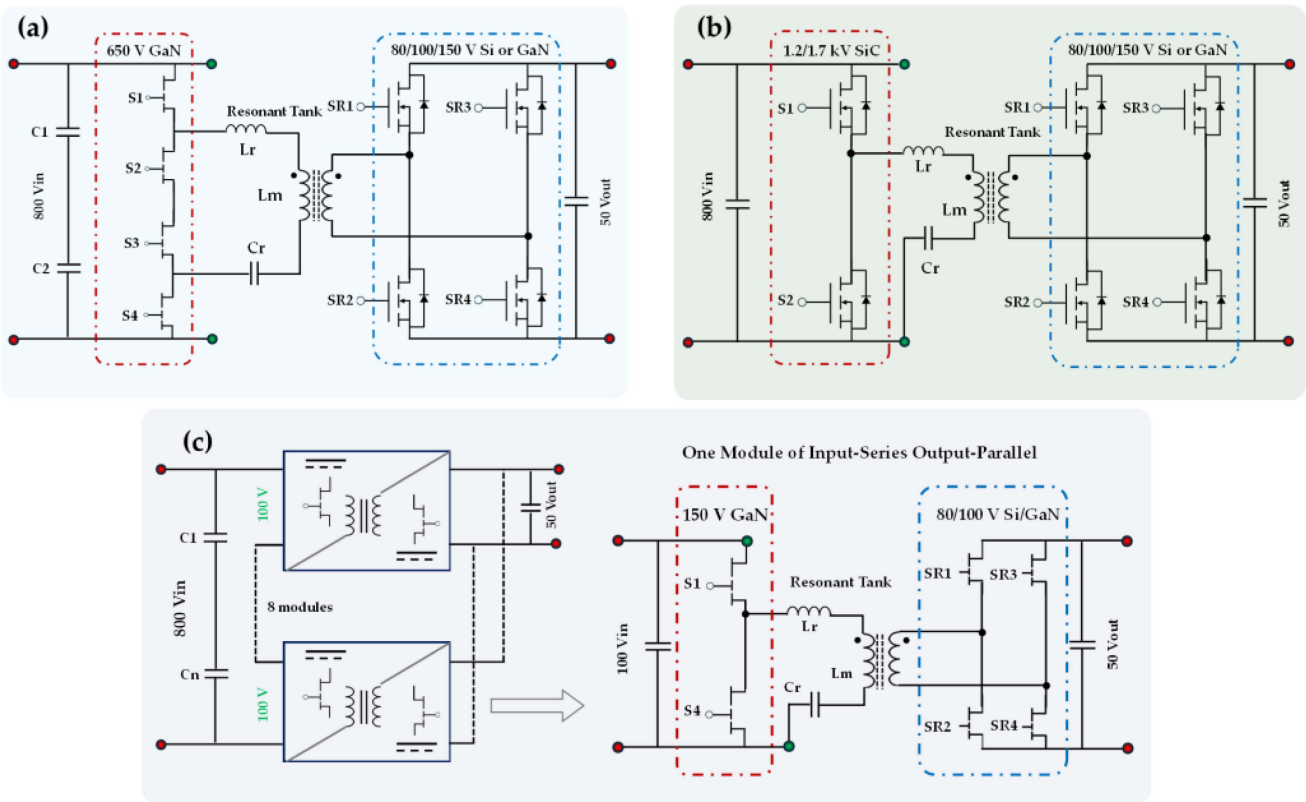


FIGURE 7. Circuit schematics of representative HVDC IBC topologies: (a) Input-series half-bridge (IS-HB) LLC, (b) Half-bridge LLC, and (c) Input-series output-parallel (ISOP) LLC converters.

low switching losses and high-frequency switching capability. However, because only half of the DC bus voltage is applied to the resonant tank during each switching cycle, the converter experiences higher current stress than full-bridge implementations, particularly at high power levels. As power levels increase, HB-LLC, FB-LLC, and ISOP-LLC topologies are adopted to distribute current and voltage stress while maintaining high efficiency and power density through soft-switching operation, as discussed in Section II-B for 800 VDC input conversion. The HB-LLC topology is illustrated in Fig. 7(b). Representative implementations in this power range include 2.5 kW, 6 kW, 10 kW, and 20 kW converters. These designs typically employ 1.2 kV and 1.7 kV SiC MOSFETs on the primary side because of their high breakdown voltage capability and low conduction losses [74]. The HB-LLC topology offers a simpler structure with fewer components and reduced control complexity, whereas the FB-LLC topology utilizes the full DC bus voltage, reducing current stress and enhancing power-transfer capability at higher power levels. However, these converters generally operate at relatively low switching frequencies (27–140 kHz), requiring larger transformers and magnetic components, which limits power density despite their high efficiency. In the ISOP topology, multiple converter modules are connected in series at the input and in parallel at the output, enabling input voltage sharing and output current sharing, as shown in Fig. 7(c). During operation, each module processes only a fraction of the total input voltage through its resonant stage, ranging from 12.5% in the 6 kW EPC implementation to 50% in the 12 kW STM design. This reduced voltage stress enables the use of 700 V, 650 V, 150 V, or 120 V GaN devices instead of the high-voltage SiC MOSFETs typically required in HB-LLC and FB-LLC converters. In addition, the use of GaN devices enables high switching frequencies (650 kHz–1 MHz), significantly reducing the size of magnetic and passive components and thereby increasing power density. Consequently, ISOP-based converters developed by STM, EPC, and Navitas achieve power densities exceeding 2100–2600 W/in^3, highlighting the strong potential of this architecture for future AI data center HVDC IBC applications. Furthermore, sharing output current improves thermal management, reduces current stress, and enhances system reliability.

B. TRADITIONAL PSU VS HVDC IBC

An analytical comparison of the compiled datasets indicates that 800 V HVDC architectures provide clear advantages in converter compactness and stage efficiency over conventional AC-distributed PSU systems. Reported 800 V HVDC IBCs achieve significantly higher volumetric power density, reaching 2100–2600 W/in^3 in 6–20 kW designs (STM, Navitas, and EPC). In contrast, conventional AC-input PSU's in the 3–12 kW range typically remain below ∼113 W/in^3, mainly due to the additional volume required for the front-end EMI filter, PFC stage, bulk capacitor, and cooling hardware. Efficiency trends further support this advantage. The surveyed AC-input PSUs report Pk efficiencies of approximately 96–98%, whereas HVDC IBC converters demonstrate comparable or slightly higher performance, reaching 98.4% in a 10-kW design despite operating at much higher switching frequencies. However, practical deployment of 800 V HVDC systems in AI data centers requires advanced protection and fault-management strategies [75], [76]. Unlike AC systems, DC networks have no natural current zero-crossing, making fault interruption more difficult and allowing persistent arcing. In addition, fault currents can rise rapidly and may reach 10–20 kA peak, as highlighted in emerging rack-scale architectures [77]. Typical fault conditions include pole-to-ground and pole-to-pole short circuits, which require extremely fast detection, often within sub-1 ms [78], [79]. Fault interruption is commonly achieved using hot-swap integrated circuits in power distribution boards, enabling microsecond-scale turn-off, inrush-current control, output discharge, and field serviceability [80]. Additional protection may be provided by solid-state circuit breakers, hybrid breaker structures, DC-rated fuses, and current-limiting reactors to reduce electrical stress on sensitive GPU loads [81]. Therefore, while 800 V HVDC architecture offers compelling benefits in efficiency, power density, and current reduction, robust system-level protection remains a key requirement for reliable deployment.

IV. ON-BOARD POWER CONVERSIONS IN AI SERVER TRAY

An AI server tray contains multiple independently controlled power domains, such as CPUs, GPUs, memory, and core logic, each requiring precise voltage and frequency regulation, typically within the range of 0.6–1.0 V [82], [83]. These domains also exhibit diverse transient load characteristics, necessitating fast and accurate dynamic response from the power supply [84]. To satisfy these requirements, modern AI servers commonly use a two-stage power delivery architecture. In this, the LV IBC performs the bulk voltage conversion from the 50 VDC rack bus to 12 VDC, reducing current levels and simplifying board-level power distribution [85]. Following, VRM provides PoL regulation, converting the 12 VDC to processor supply voltages of approximately 0.7–1.8 VDC while meeting the demanding transient response requirements [86]. As AI processors continue to demand higher currents, achieving high efficiency and power density across the LV IBC and VRM stages has become increasingly challenging. Although direct conversion from the rack bus to the processor voltage can theoretically improve overall system efficiency by eliminating intermediate stages and associated PDN losses [87], the required conversion ratio of nearly 50:1 presents significant design challenges. Recent advances in WBG semiconductors, high-frequency magnetics, and integrated power architectures have renewed interest in such single-stage solutions. Therefore, this section comparatively reviews LV IBCs (50 V to 8–12 V), VRMs (12 V to PoL), and direct 50 V-to-PoL converters in terms of output power and current capability, efficiency, power and current density, converter topologies, semiconductor technologies, and suitability for next-generation AI server trays.

TABLE 5. Key Specifications of LV IBC 50 V in to 12 Vout From Academic Industrial Institutes

Ref	Vin – Vout	Power [W]	Density [W/in³]	Pk Eff. [%]	FL Eff. [%]	Freq [kHz]	Volume L×W×H	Topology	Semi
EPC [88]	48 / 12	300	723	95.5	95.4	500	33×22.9×9	2-Φ Buck	100 V GaN
Zhejiang [89]	40–60 / 12	360	480	97.3	96.1	1000	44.5×33.8×8.2	DC-T	100 & 30 V Si
Infineon [90]	40–60 / 10–15	400	3060	97.1	96.0	1150	7×51	ZVS SC	40, 35 & 25 V Si
NDSU [91]	54–60 / 10	450	750	98.6	97.2	387	61×27×6	ReSC	30 V GaN
Infineon [92]	36–75 / 12	600	360	95.6	95.1	250	36.8×58	FB-FB	100 & 40 V Si
EPC [93]	48 / 12	600	1000	96.2	95.8	500		M-Φ Buck	100 V GaN
Flex [94]	36–75 / 12	600	346.6	96.4	95.8	180	58.4×36.8×13.2		
Univ. Illinois [95]	36–60 / 12	600	2180	98.9	98.0	121	35×11.7×5.5	ReSC	40 & 30 V Si
Flex [96]	40–60 / 12	700	472.2	96.4	96.1	400	57.9×36.8×11.4		
Delta [97]	40–60 / 12	700	329.5	97.7	97.5	800	58.4×36.8×16.2		
UC Berkeley [98]	48 / 12	720	2500	99.0	97.2	100	35×11.7×5.6	ReSC	40 & 30 V Si
Delta [99]	40–60 / 12	800	420.7	97.5	97.4	800	58.4×36.8×14.5		
Flex [100]	36–60 / 12	800	421.3	96.7	96.9	230	58.4×36.8×14.5		
MPS [101]	40–60 / 10–15	800	3310	98.1	96.5		24×18×9.1	LLC + Buck	
Queen's [102]	40–60 / 12	840	2500	99.1	97.2	60		ZIV	40 & 25V Si
Reed [103]	40–60 / 12	860	516.3	98.3			58.4×36.8×12.7		
Flex [104]	40–60 / 12	900	563	96.8	96.9	230	58.4×36.8×12.2		
EPC [105]	36–60 / 9–15	1000	1227	97.5	96.7	1000	22.9×58.4	LLC	100 & 40 V GaN
Flex [106]	40–60 / 8–12	1000	625.5	97.3	96.8	230	58.4×36.8×12.2		
Delta [107]	40–60 / 12	1000	508	97.3	97.2	1100	58.4×36.8×15		
Reed [[108]	40–60 / 10–15	1000	5118	98.1			23×17.4×8		
EPC [109]	48 / 12	1000	5130	98.0	96.2	1600	17.5×22.8×9	LLC	100 & 40 V GaN
Infineon [110]	48 / 12	1100	564	97.3	98.4	600		ZVS SC	80, 40 & 25 V Si
TI [111]	48 / 12	1100	466	98.0	96.8		36.8×58.4×18	2-Φ Buck	100 V GaN
TI [112]	48 / 12	1100	1300	97.8	95.5	1000	22.9×58.4×10.2	LLC-DCX	100 V GaN
EPC [113]	40–60 / 10–15	1200	1472	97.3	96.3	1000	22.9×58.4	LLC	100 & 40 V GaN
Delta [114]	40–60 / 12	1300	660.8	97.2	96.9	1100	58.4×36.8×15		
Flex [115]	40–60 / 12	1300	683.6	97.2	96.6	180	58.4×36.8×14.5		
Reed [116]	40–60 / 12	1300	780.5	98.3			58.4×36.8×12.7		
Infineon [117]	40–60 / 10–15	1300	3700	98.3	97.8	300	40×18×8	SHSC	80 & 40 V Si
Flex [118]	48–56 / 12	1400	773.6	97.5	96.9	180	58.4×36.8×13.8	~	~
Reed [119]	40–60 / 12	1600	960.6	98.3			58.4×36.8×12.7	~	~
TI [120]	48 / 12	2000	847.2	98.2	97.5		36.8×58.4×18	4-Φ Buck	100 V GaN
Flex [121]	40–60 / 12	2000	1051.7	97.9	97.7	180	58.4×36.8×14.5		
Reed [122]	40–60 / 12	2000	1097.1	98.0	98.0		58.4×36.8×13.9		
EPC [123]	48 / 12	2000	104	96.5	96.0	500	112×70×40	M-Φ Buck	100 V GaN

A. 50 V TO 12 V LOW-VOLTAGE INTERMEDIATE BUS CONVERTERS

Table 5. presents a broad range of LV IBC designs from both academic and commercial sources, covering a 12 V output and power levels from 300 W to 2000 W. At low power levels (300–1100 W), 50 V-to-12 V converters achieve very high efficiency because due to limited conduction losses in rectifiers, transformer windings, and interconnects. The 720 W ReSC converter achieves 99.0% Pk and 97.2% FL efficiency. Queen's University's 2-Φ ZIV converter (840 W) achieves the highest Pk efficiency in the dataset at 99.1%, while the EPC LLC converter (1000 W, GaN) and TI 2-phase buck converter (1100 W, GaN) both maintain Pk efficiencies of approximately 98%. At power levels of 1.2–1.6 kW, EPC LLC converter (1200 W, GaN) achieves 97.3% Pk efficiency, while the Infineon SHC (1300 W) reports 98.3% Pk and 97.8% FL efficiency, exhibiting the smallest efficiency drop among the designs in this power range. Commercial quarter-brick modules from Delta and Flex maintain 96.5%–97.0% FL efficiency. At very high power levels (1.6–2.0 kW),

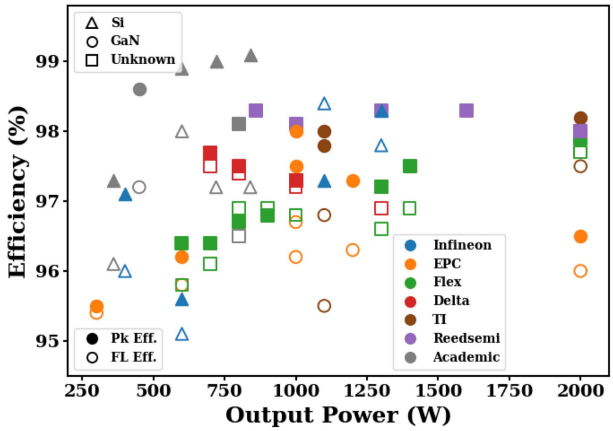


FIGURE 8. Output power vs efficiency of reported LV IBC 50 V-to-12 V designs.

high Pk efficiency remains achievable. The Reed converters rated at 1600 W and 2000 W achieve Pk efficiencies of 98.3% and 98.0%, respectively, while the TI 4-Φ buck converter (2000 W, GaN) achieves 98.2% Pk and 97.5% FL efficiency. Although efficiencies above 98% remain achievable, the gap between Pk and FL efficiency generally slightly widens with increasing power. Consequently, the practical FL efficiency ceiling decreases from approximately 98% at sub-800 W power levels to around 96.0%–97.5% at 1.3–2.0 kW. Fig. 8 shows the relationship between output power and efficiency.

Fig. 9(a) shows the relationship between power density and output power. At low power levels, custom-packaged academic and GaN-based converters achieve the highest relative densities. The SC and ReSC converters achieve power densities of 3060 W/in^3 and 2500 W/in^3, respectively, dominating the density frontier below approximately 1 kW. Furthermore, the EPC GaN LLC converter (1000 W) achieves the highest overall density at 5130 W/in^3, while the Reed converter (1000 W) reaches 4095 W/in^3. The SHC (1300 W) attains 3700 W/in^3. At higher power levels, custom-packaged designs show a clear decline in power density from the peak achieved near 1 kW, whereas fixed-footprint commercial modules continue to scale within the quarter-brick constraint. Delta reaches approximately 916 W/in^3 at 1600 W, while Flex and Reed achieve maximum densities of 1052 W/in^3 and 1098 W/in^3, respectively, at 2 kW. In contrast, the TI and EPC designs report substantially lower power densities 847 W/in^3 and 104 W/in^3, respectively.

Fig. 9(b) shows the relationship between switching frequency and power density. Converters operating at relatively low frequencies (60–250 kHz) are generally limited to moderate power densities of approximately 300–2500 W/in^3. In contrast, converters operating in the MHz range generally occupy the power-density frontier, with several designs exceeding 3000 W/in^3 and the highest-density implementation reaching 5130 W/in^3.

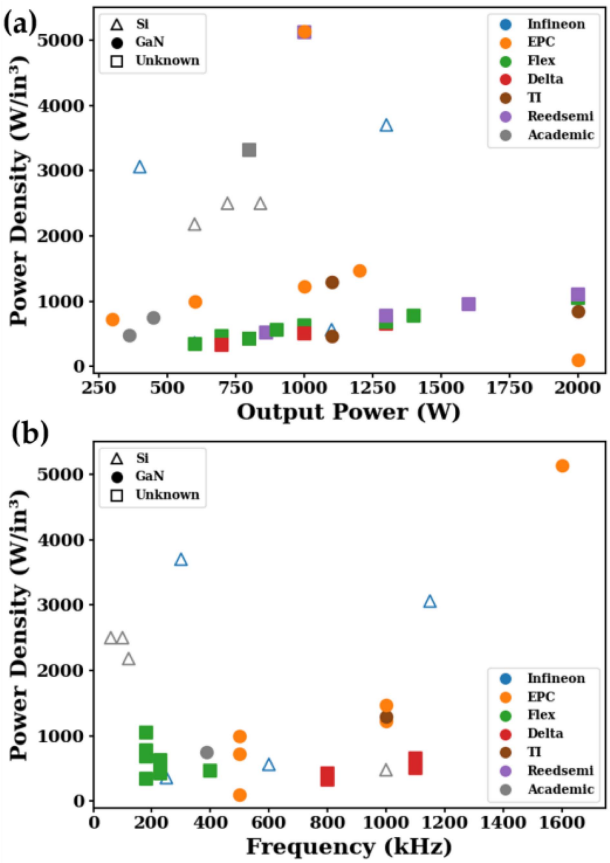


FIGURE 9. (a) Output power vs power density and (b) switching frequency vs power density of reported LV IBC 50 V-to-12 V designs.

This trend reflects the fundamental physics of magnetic energy storage, where the required inductance decreases approximately inversely with switching frequency for a given ripple-current specification. As a result, higher switching frequencies significantly reducing converter volume and increasing power density [124], [125]. Nevertheless, the results indicate that switching frequency alone does not fully determine power density. For example, an EPC GaN converter operating at approximately 500 kHz achieves only 104 W/in^3 at 2 kW output power, whereas the SHC achieves 3700 W/in^3 at 1300 W while operating at only 300 kHz. These results demonstrate that switching frequency is only one of several factors influencing converter volume and power density. Consequently, Fig. 9(b) demonstrates a clear positive correlation between switching frequency and power density, while also indicating that frequency scaling alone is insufficient to fully explain the observed density variations.

The surveyed LV IBC designs for 50 V-to-12 V conversion fall into three main topology families: SC and resonant variants, LLC resonant converters, and synchronous buck converters, each representing different trade-offs among efficiency, power density, and scalability. Fig. 10 presents three representative circuit schematics along with the types

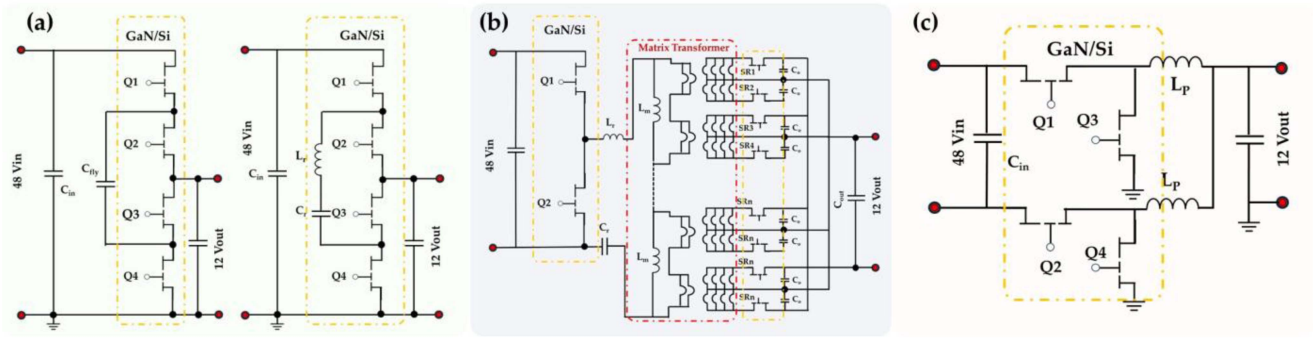


FIGURE 10. LV IBC circuit topologies: (a) Switched-capacitor (SC) and resonant SC; (b) half-bridge LLC with matrix transformer and (c) 2-phase synchronous buck converter.

of power devices employed. SC converters operate by periodically reconfiguring capacitor–switch networks between charge and discharge states, transferring energy via charge redistribution among flying capacitors arranged in series–parallel configurations [126], [148]. This approach eliminates magnetic energy storage, thereby removing transformer core losses and significantly reducing passive component volume. However, conventional hard-switched SC converters suffer from charge redistribution loss caused by instantaneous current spikes when capacitors at different potentials are directly connected, which limits efficiency. To overcome these limitations, ReSC converters introduce small series inductors to shape the charge-transfer current into a sinusoidal waveform, enabling natural ZCS [151], which explains why ReSC implementations occupy the efficiency frontier in Fig. 8. The LLC converter family represents the most widely adopted isolated topology, exploiting resonant tank operation to achieve ZVS and ZCS [58], [62]. In 50 V-to-12 V applications, the inherent transformer ratio closely aligns with the required 4:1 conversion, enabling both high efficiency and compact magnetic design. The matrix transformer extension further improves performance by distributing flux across multiple planar cores, reducing core loss and AC resistance [142]. These characteristics make matrix-transformer LLC converters particularly attractive for high-density AI server power delivery [66]. In contrast, synchronous buck converters provide a non-isolated solution, typically implemented in interleaved multiphase configurations. By phase-shifting parallel stages (e.g., 180° in two-phase and 90° in four-phase systems), the effective ripple frequency increases, enabling smaller output filters while maintaining manageable device stress [32], [127]. Unlike SC and LLC converters, buck converters use direct PWM regulation, providing excellent controllability and scalability without the complexity of resonant tank design [167]. The interleaving mechanism also distributes current among multiple phases, reducing RMS current stress in individual devices and helping maintain high efficiency at output powers approaching 2 kW.

Fig. 11 shows the relationship between output power and operating temperature across Si and GaN-based converter implementations. Si-based converters exhibit a general upward

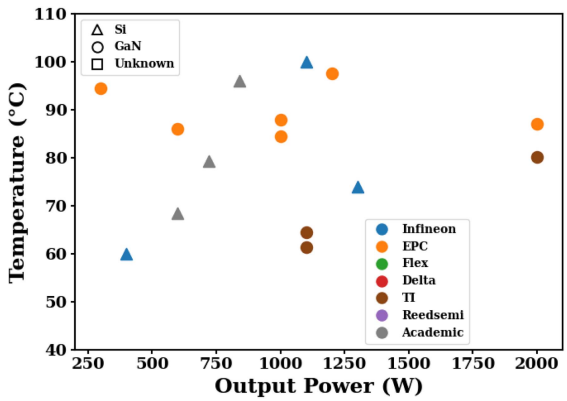


FIGURE 11. Operating temperature vs output power of 15 reported LV IBC 50 V-to-12 V designs.

trend in operating temperature with increasing output power, reflecting the growing thermal stress imposed on the system as power levels scale. In contrast, GaN-based converters consistently operate at elevated temperatures regardless of output power level, with most implementations reporting temperatures in the range of 84–98°C across the 300 W to 1.2 kW range. This persistently high thermal behavior in GaN systems is attributed to the compact, high-density packaging typical of GaN-based designs, which concentrates heat dissipation within a limited footprint and challenges heat removal even at moderate power levels.

The distinction between the two device technologies underscores the fundamental difference in their thermal characteristics: while Si-based designs benefit from more mature and distributed thermal management strategies that allow operating temperature to scale more gradually with power, GaN-based designs demand more aggressive cooling solutions to sustain reliable operation. These results indicate that thermal performance is governed not only by output power but also by the interplay between device technology, topology, packaging, and cooling strategy [109], [110], [128].

TABLE 6. Key Specifications of VRM 12 V in to PoL From Academic Industrial Institutes

Ref	Vin / Vout	Iout (A)	Density (A/mm²)	Pk Eff. (%)	FL Eff. (%)	Freq (kHz)	Volume [mm] L x W	Topology	Semi
Zhejiang [129]	16 / 0.6–1.6	5	1.30	94.5	84.4	1000	1.965 x 1.965	DP Series-Cap	180 nm Si BCD
Macau [130]	12 / 0.6–1.2	5	0.56	91.8	75–80	800	2.96 × 3	ReSC-PL	180 nm Si BCD
USTC [131]	12 / 1–1.8	5	1.0	92.2	84	1000	2 × 2.5	hybrid-CCP	180 nm Si BCD
SCUT [132]	12 / 1.0–1.8	5		93.8	84	1000	~	TP Series-Cap	180 nm Si BCD
Sogang [133]	12 / 1.0–1.8	5	0.52	91	78	500	1.940 x 5	MDHC	~
SYSU [134]	12 / 0.8–1.8	8	1.51	90.9	79.2	2000	1.70 × 3.11	SC-MO	180 nm Si BCD
TI [135]	14 / 1.0–1.8	10	0.71	82.5	78	5000	3.5 × 4	2-Φ Series-Cap	Monolithic Si MOS
Princeton [136]	24 / 0.5–1.2	55	0.057	88	76	281 & 1266	32 × 30 (PCB)	LEGO	Si MOS
NYCU [137]	12 / 1.0	100	0.34	93.6	80	1000	12 × 12	IP-TLVR	180 nm Si BCD
Auburn[138]	12 / 1	105		96	90	2000		5-Φ Buck	GaN
Infineon [139]	16 / 0.2–3	160				2000			Si MOS
AD [140]	12 / 1.0	180	5.28/Φ	92.5		400	2.540 x 2.235	6-Φ Buck	600 nm BiCMOS
DP S.L. [141]	12 / 0.5–1.2	500		97	95	150		M-Φ DPC	GaN & Si

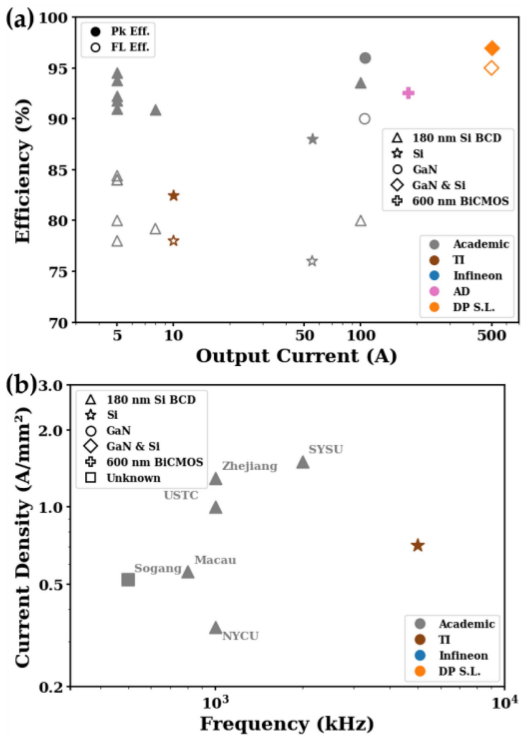


FIGURE 12. (a) Output current vs efficiency and (b) switching frequency vs current density of reported VRM 12 V-to-PoL designs.

B. 12 V TO POL VOLTAGE REGULATION MODULES

Table 6. summaries VRMs from both academic and commercial sources, covering output voltages of 0.6-1.8 V and output currents from 5 to 500 A. Fig. 12(a) shows the relationship between output current and efficiency. Among low-current (5–10 A) academic Si Bipolar-CMOS-DMOS (BCD) designs, Pk efficiencies of 90.9–94.5% drop by 10–14 percentage points at FL. As output current increases to 55–105 A, a clear semiconductor technology and topology driven divergence emerges. Princeton's 55 A Si-based 2-stage design achieves only 88% Pk and 76% FL efficiency due to cumulative losses from cascaded conversion stages. In contrast, Auburn's 105 A GaN-based 5-Φ buck converter reaches 96% Pk and approximately 90% FL efficiency, outperforming even the low-current Si BCD designs. This result indicates that converter architecture and semiconductor technology can have a greater influence on efficiency than output current alone. At the highest current level, Differential Power S.L.'s (DP S.L.) 500 A GaN multi-Φ direct power converter (M-Φ DPC) achieves the highest efficiency in the survey at 97% Pk and 95% FL, demonstrating the ability of GaN-based M-Φ direct conversion to maintain high efficiency even at extreme current levels. While efficiency remains a key performance metric, VRMs must also deliver hundreds of amperes within the limited area available near modern processors, making current density an equally important figure of merit, [85], [86]. The relationship between current density and switching frequency is shown in Fig. 12(b). Among the academic Si BCD designs, a moderate positive correlation exists between switching frequency and current density. Current density increases from 0.52 A/mm^2 at 500 kHz (Sogang) to 1.51 A/mm^2 at 2 MHz (SYSU), with Zhejiang, USTC, and Univ. Macau following the same trend. However, NYCU's 1 MHz inverted-pyramid trans-inductor voltage regulator (IP-TLVR) highlights the importance of integration strategy beyond switching frequency alone. When the required off-chip trans-inductors are included, the system-level current density decreases to approximately 0.34 A/mm^2,

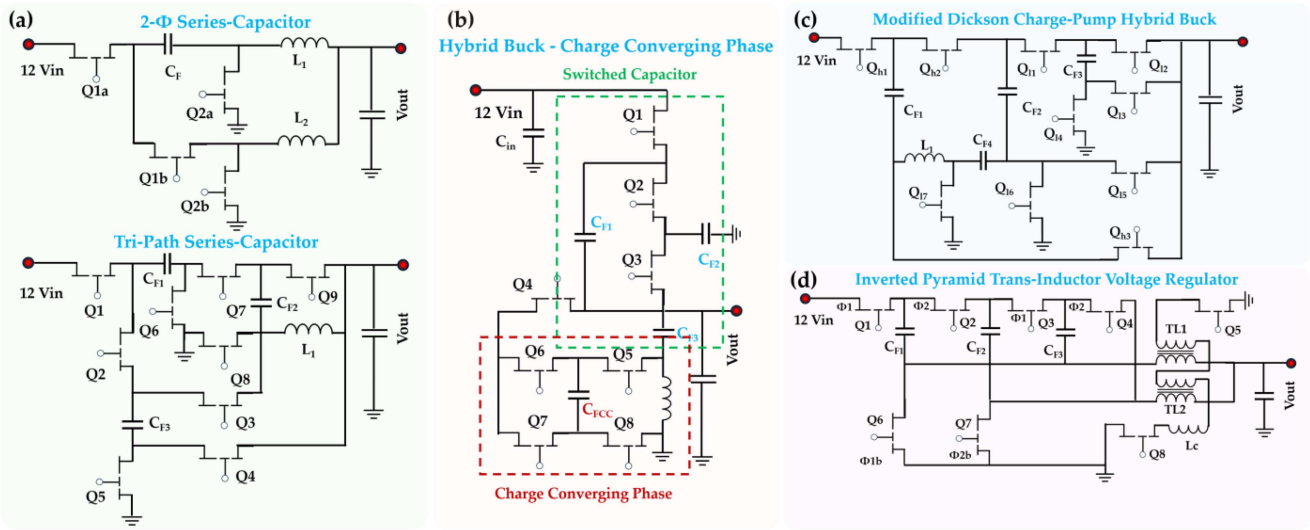


FIGURE 13. 12 V-to-PoL VRM circuit topologies: (a) 2-Φ series-capacitor and Tri-path series-capacitor; (b) Hybrid buck with charge converging phase; (c) modified dickson charge-pump hybrid buck (MDHC) and (d) Inverted pyramid trans-inductor voltage regulator (IP-TLVR).

indicating that the design prioritizes 100 A capability and transient performance over integration density. At the LF extreme, M-Φ DPC's 150 kHz design achieves the lowest system-level current density (0.149 A/mm^2), illustrating the density penalty associated with LF operation and high output-current capability.

The surveyed 12-V-to-PoL VRMs are categorized into four single-stage topology families: capacitor-based (Series-Capacitor, SC, and ReSC), hybrid (hybrid buck-CCP and MDHC), transformer-based (IP-TLVR and M-Φ DPC), and multiphase buck, together with the two-stage LEGO architecture. The capacitor-based family dominates the 5–10 A range. As shown in Fig. 13(a), the 2-Φ series-capacitor converter shares a single flying capacitor between two interleaved buck phases, with the capacitor connected in series with Φ-A and supplying the high-side switch of Φ-B instead of directly from V in. The dual-path (DP) series-capacitor converter extends this concept by replacing the second interleaved phase with a single inductor and a capacitor ladder that creates a second capacitive current path to the output. The tri-path (TP) series-capacitor converter further extends this principle by employing a single inductor and three flying capacitors to establish three parallel current paths, thereby reducing the inductor current and extending the duty-cycle range to full-range operation. The ReSC converter has been discussed in the previous section. The ReSC-PL adds a small resonant capacitor–inductor branch in parallel with the main inductor, allowing part of the output current to bypass the main inductor and reducing its average current to approximately half of the load current. Unlike the ReSC-PL, the SC-MO converter shares flying and DC capacitors across multiple series-connected hybrid cells, each with its own inductor, enabling independently regulated multi-output operation. The hybrid buck with CCP extends the SC principle by introducing a dedicated charge-converging capacitor (CFCC), which is charged simultaneously by the inductor and two flying capacitors throughout an entire switching phase, rather than during only part of the switching period in earlier dual-path designs, as shown in Fig. 13(b). During the subsequent phase, the CFCC discharges its accumulated charge directly to the output. The MDHC, shown in Fig. 13(c), converts a conventional charge pump into a hybrid capacitor–inductor topology by adding an inductor, a flying capacitor, and a switch while removing one original switch. The inductor carries part of the output current, whereas the flying capacitors transfer charge throughout most of the switching cycle, reducing the average inductor current. The MDHC is readily scalable by increasing the number of capacitor stages (N), further reducing the inductor current for a given input-to-output voltage ratio. The IP-TLVR combines flying-capacitor voltage division with magnetically coupled trans-inductors, which behave as conventional inductors under steady-state conditions but couple current between phases during load transients, thereby increasing the inductor current slew rate and improving transient response, as shown in Fig. 13(d). The M-Φ DPC comprises four interleaved direct power converter cells, each incorporating a transformer. Within each cell, all switches operate synchronously, providing a near-continuous transformer current that self-resets through resonance to achieve ZVS and ZCS. The four interleaved cells share the output current, reducing ripple and enabling high-current operation. As the output current increases, multiphase architecture becomes the preferred solution. The M-Φ buck architecture scales the output current by paralleling identical buck phases, each with its own inductor and operating with equal phase offsets into a shared output capacitor, as shown in Fig. 17(b).

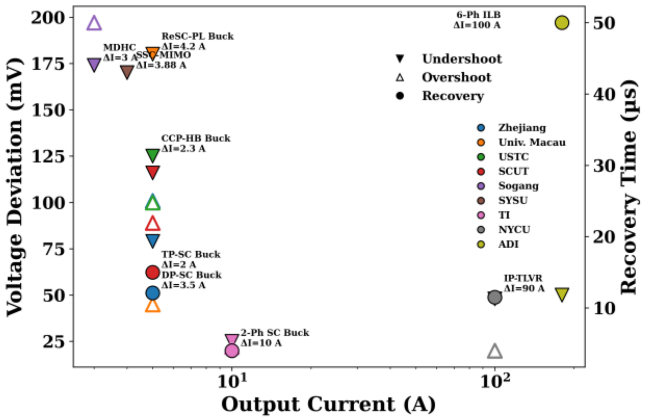


FIGURE 14. Transient performance versus output current comparison of reported 12 V-to-PoL designs.

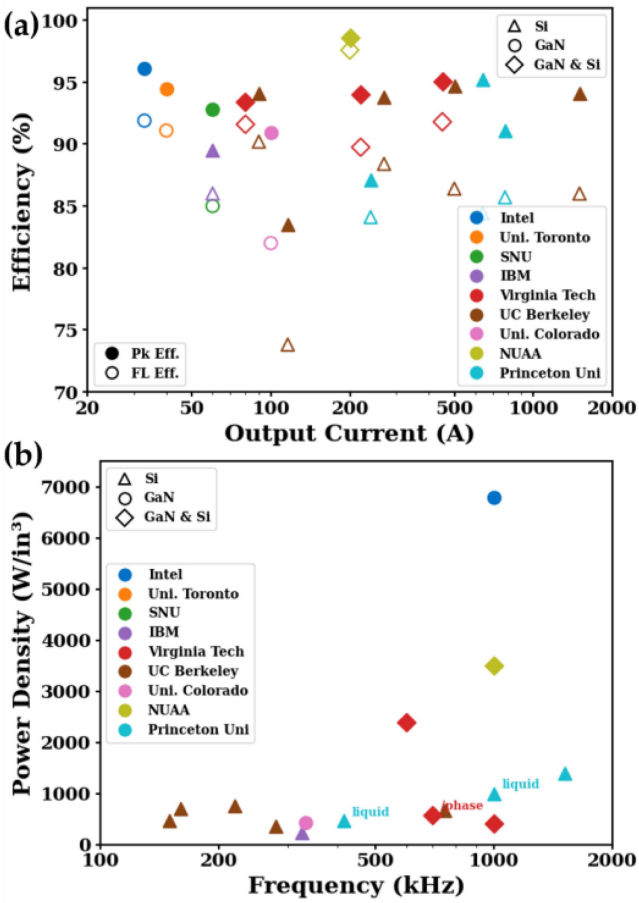


FIGURE 15. (a) Output current vs efficiency and (b) Switching frequency vs current density of reported LV IBC 50 V-to-PoL designs.

Finally, the LEGO converter employs a two-stage architecture comprising a 2:1 SC front end followed by M-Φ buck units, as shown in Fig. 17(c). Separating the SC stage for voltage conversion from the buck stage for current delivery and regulation enables multiple independently regulated output rails and scalable output power through the number of buck phases, at the expense of an additional conversion stage.

The temperature and power relationship is not included for the 12 V-to-PoL VRM dataset because operating temperature is not consistently reported across the surveyed designs. Fig. 14 shows transient performance comparisons of the reported VRM 12 V-to-PoL designs. Several implementations do not report transient metrics, while some studies report only output ripple and simulation results. After normalizing voltage deviation by load-step magnitude, Analog Devices and NYCU achieve the best reported performance at 0.50 and 0.53 mV/A, respectively, followed by TI's monolithic 2-Φ series-capacitor buck at 2.5 mV/A. The remaining capacitor-based designs exhibit substantially larger deviations, ranging from 22.6 to 58 mV/A. Three mechanisms primarily govern this ranking. First, switching frequency strongly influences control-loop bandwidth [84], [142]: TI's 5 MHz design achieves a 4 µs recovery time, whereas Analog Devices' 400 kHz multiphase buck requires 50 µs despite its small, normalized voltage deviation, highlighting that recovery time and voltage deviation are complementary transient metrics. Second, flying-capacitor charge redistribution limits the transient response of SC-buck converters, leading to larger normalized deviations at lower switching frequencies. Third, IP-TLVR uses magnetic trans-inductor coupling to enhance current slew rate during load transients [143] achieving near-best-in-class performance at only 1 MHz without aggressive frequency scaling. Overall, high switching frequency is most effective for low-current VRMs, whereas magnetic coupling and advanced multiphase architectures become increasingly important at higher currents, where current slew capability rather than control bandwidth is the primary limitation.

C. 50 V TO POL V LOW-VOLTAGE INTERMEDIATE BUS CONVERTERS

Table 7. summarizes single-stage 50 V-to-PoL converters from academic and commercial sources, covering output voltages of 0.5–7.5 V and output currents from 33 A to 1500 A. Unlike conventional 50 V-to-12 V and VRM solutions, these converters must combine a high conversion ratio with high output current, making efficiency highly sensitive to current scaling.

Fig. 15(a) shows the relationship between output current and efficiency. A clear trade-off exists between output current capability and FL efficiency across the 50 V-to-PoL converters surveyed. At the lower end of the output current levels, converters delivering 40–80 A, such as the XQSD buck and Sigma converter, achieve FL efficiencies of 91.1% and 91.6%, respectively, with a narrow Pk-to-FL efficiency drop of only 3–4%. As output current increases into the hundreds of amps, this gap widens considerably. The VIB (640 A) and LEGO

TABLE 7. Key Specifications of Direct LV IBC 50 V in to PoL From Academic Industrial Institutes

Ref	Vin/ Vout	Iout (A)	Density (W/in³)	Pk/FL Eff. (%)	Freq (kHz)	Volume (LxWxH)	Topology/ No. stages	N	Semi	Semi Cost/Iout
Intel [144]	48/ 6	33	6800	96.1 91.9	1000		SS-SC Single	4	40 V GaN	
Toronto [145]	48/ 1	40		94.5 91.1	125	50x41	XQSD Single	2	100 & 40 V GaN	1.23
UCB [146]	48/ 6	40	1675	98.6 96	70	35x11.7x5.5	Multi ReSC Single	1	40 & 25 V Si	0.66
UCB [147]	48/ 4	60	1154	97 94	72	65x11.2x5.6	ReSC Two	1	40 & 25 V Si	0.63
SNU [148]	48/ 1	60		92.8 85	440	60x40	3L-HB CD Single	2	40 & 25 V GaN	
IBM [149]	48/ 1	60	230.8	89.5 86	325		ACF Single	1	100 V Si	
VT [150]	48/ 1	80	420	93.4 91.6	1000 600	40x20x4	Sigma Single	4	100 & 40 V GaN 5 V Si	0.64
UCB [151]	48/ 2	90	702	94.1 90.2	160	18x16x6.2	CaSP Two	3	40 & 25 V Si	0.45
Colorado [152]	48/ 1–5	100	440	90.9 82	333		DP-MIH Single	2	40 & 30V GaN	1.32
UCB [153]	48/ 1–3	116	663	83.5 73.8	750	25.8x31x3.6	SDIH Single	2	25 & 40 V Si	0.46
NUAA [154]	48/ 5–7.5	200	3500	98.6 97.6	1000	45x22.9	Hybrid ReC Single	3	100 V GaN 25 V Si	0.24
UniBo [155]	48/ 4	200	330	92 85	33 100	58x22.8x30	Dual bus Two	3+1	80 & 25 V Si	0.73
VT [156]	48/ 1	220	576/Φ	94 89.8	700	34x26.5	FB-HT CD Single	4	100 V GaN 40V Si	0.19
Princeton [157]	48/ 1	240	1390	87.1 84.1	1515	30x11x8.4	Mini-LEGO Two	12	Si	0.39
UCB [158]	48/ 1–1.5	270	360	93.8 88.4	280	75x25x6.4	Dickson[2] Two	9	40 & 25 V Si	0.45
VT [159]	48 / 1.8	450	2400	95.1 91.8	600	100x10x5.8	HB-LLC Single	14	100 V GaN 15 V Si	0.27
UCB [160]	48/ 1	500	464	94.7 86.4	150	82x30x7.3	Hybrid SC Two	16	40 & 25 V Si	0.40
Princeton [161]	48/ 0.8–1.2	640	463 (liquid)	95.2 84.4	100 417	66x43.8	VIB Two	16	40 & 25 V Si	0.13
Princeton [162]	48/ 0.8–1.5	780	1000 (liquid)	91.1 85.7	286 1000	46x16x16	LEGO Two	12	25 V Si	0.22
UCB [163]	48/ 1	1500	759	94.1 86	220	202x26x6.2	Hybrid SC Two	40	40 & 25 V Si	0.35

* *N: Number of series/modules/phases sharing output current*

(780 A) achieve FL efficiencies of 84.4% and 85.7%, respectively, while the 1500 A hybrid SC converter exhibits a rise in conduction-loss contribution from 13.4% at Pk efficiency to 32.7% at FL. Two notable exceptions deviate from this trend. The hybrid ReC achieves the highest reported FL efficiency of 97.6% at 200 A, whereas the SDIH converter reaches only 73.8% at 116 A, largely due to its high per-phase current of 52.5 A. Despite severe current-scaling challenges, high-current designs such as Dickson^2 and Mini-LEGO maintain FL efficiencies of 84%–88% while operating at high output currents. Nevertheless, the efficiency improvement achievable at very high output currents remains limited, making reduced efficiency an inherent challenge in single-stage power conversion.

Fig. 15(b) confirms the positive frequency–density correlation, across the 50 V-to-PoL converter range. At the lower end of the frequency spectrum, the hybrid SC 500 A and 1500 A converters operate at 150–220 kHz and achieve power densities of 464–759 W/in^3, as the large inductance required at these frequencies remains a significant volume constraint. As the switching frequency increases to the 600–1000 kHz range, the FB-HT CD and sigma converters achieve power densities of 576 W/in^3 per phase and 420 W/in^3, respectively, benefiting from reduced magnetic component size. Notably, HB-LLC DCX achieves 2400 W/in^3 at only 600 kHz, demonstrating that high power density is achievable without aggressive frequency scaling. The hybrid ReC achieves 3500 W/in^3, one of the highest reported power densities at 1 MHz. At the highest frequencies, LEGO (1 MHz) and Mini-LEGO (1.515 MHz) achieve the highest reported power densities among 1 V-output designs, reaching 1000 W/in^3 and 1390 W/in^3, respectively. The absolute density ceiling in the survey is set by on-package SS-SC IBC, which achieves 6800 W/in^3 at 1 MHz (6 V-output), representing a significant outlier relative to board-level implementations.

Table 7 reveals a clear tradeoff among efficiency, output current capability, and power density, indicating that no single topology family simultaneously optimizes all three metrics. Accordingly, the reported topologies are categorized into single-stage and two-stage architectures, implemented through SC, SCB, Multi-Φ interleaved buck, interleaved CP, hybrid, and transformer-based converters. Capacitor-based topologies, including SS-SC, ReSC, and Multi-ReSC converters, are summarized in Table 7. As discussed in Section IV-A, the SC and ReSC converters, illustrated in Fig. 10(a), operate by periodically reconfiguring capacitor–switch networks to transfer energy through charge redistribution among flying capacitors arranged in series–parallel configurations. The SS-SC converter achieves an 8:1 voltage step-down by connecting four identical 2:1 SC modules in series across the 48-V input. Extending this concept, the Multi-ReSC converter introduces additional switching phases within each switching cycle, enabling a single augmenting inductor to resonantly soft charge all flying capacitors at different resonant intervals. This approach achieves a higher conversion ratio while reducing the required number of switches and flying capacitors. Hybrid converters integrate a flying capacitor ladder with inductors connected to intermediate switching nodes rather than a single output node. The hybrid topologies summarized in Table 7 include the XQSD, SDIH, and DP-MIH converters. As shown in Fig. 16(a-i), the XQSD combines a series-capacitor with a symmetric 2-inductor buck stage. Cross-coupled charge/discharge paths provide passive capacitor-voltage and inductor-current balancing while reducing the switching-node voltage by a factor of four, thereby lowering component count and device voltage stress. The SDIH converter, shown in Fig. 16(a-ii), combines two DIH cells operating 180° out of phase. By merging redundant switch pairs and paralleling inductors, it reduces the switch count by two while requiring only two inductors, achieving a component count comparable to a single DIH cell. The DP-MIH converter, shown in Fig. 16(a-iii), employs a flying-capacitor ladder connected to the input, with inductors coupled to each intermediate switching node and paralleled at the output. Through dual-phase interleaved operation, the inductors act as current sources to resonantly soft-charge the flying capacitors, providing inherent capacitor-voltage balancing and inductor-current sharing without requiring split-phase control. Transformer-based topologies, including 3L-HB CD, ACF, Sigma, Hybrid-ReC, FB-HT CD, and HB-LLC converters, are summarized in Table 7. The 3L-HB CD converter, shown in Fig. 16(b), employs a three-level half-bridge primary with a flying capacitor generating a V in/4 transformer voltage, reducing switch voltage stress and switching losses. Its secondary current-doubler rectifier with an untapped winding and two interleaved inductors provide current sharing, ripple cancellation, and reduced winding losses. The ACF converter, shown in Fig. 16(c), uses a single-switch PWM clamp structure to drive a 12:1 transformer, where the clamp circuit resets magnetizing energy and reduces stress. The Sigma topology integrates an LLC-DCX and buck converter in an input-series output-parallel configuration, with the LLC stage processing most of the power through soft switching while the buck stage provides regulation and transient response. The Hybrid-ReSC bus converter combines a switched-capacitor network with matrix-integrated transformers, using LLC resonant tanks to achieve fixed-ratio 8:1 DCX operation with ZVS and reduced magnetic volume. The FB-HT CD converter uses a half-turn transformer secondary and current-doubler rectifier to reduce winding loss and enable high-current operation. The HB-LLC DCX topology employs an LLC resonant tank to achieve ZVS and ZCS, as discussed in Section II-B.

Two-stage architectures partition the overall 48:1 conversion ratio between a front-end stage that performs efficient, typically unregulated, bulk voltage step-down and a second stage that provides output regulation and high-bandwidth transient response. This approach relaxes the voltage stress, duty-cycle, and magnetic design constraints of each stage. The implementations summarized in Table 7 include SC front ends cascaded with SCB modules (Dickson^2 and Hybrid-SC), SC front ends followed by multi-Φ buck converters (LEGO and CaSP), a cascaded two-stage ReSC converter, an interleaved

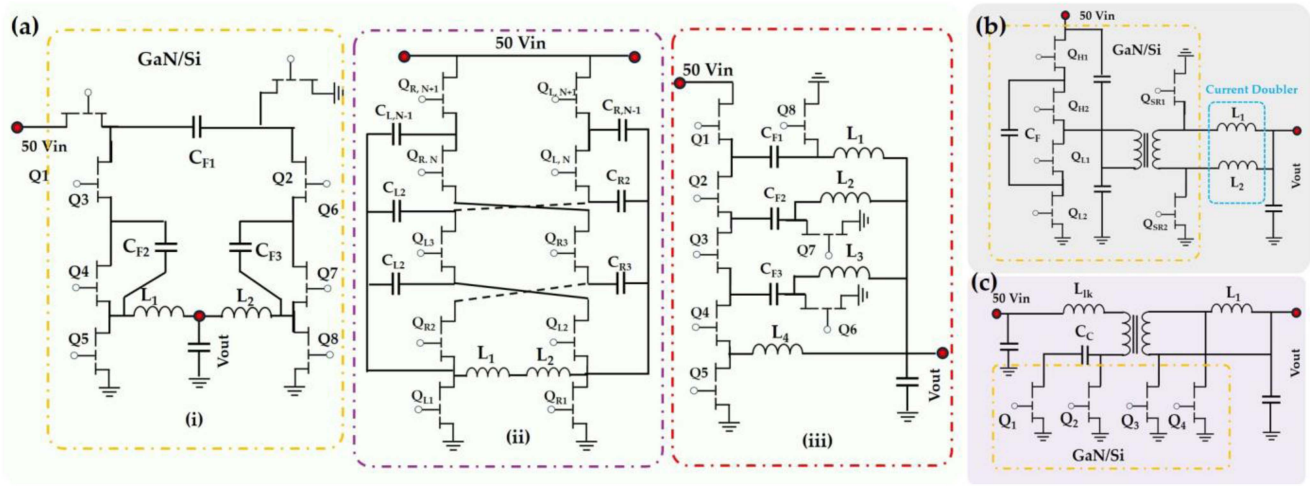


FIGURE 16. 50 V to PoL circuit topologies: (a) Cross-coupled series-capacitor quadruple converter, sym 2-inductor hybrid converter and 2-Φ multi-inductor hybrid converter; (b) HB converter with current-doubler rectifier; and (c) Active-clamp forward converter.

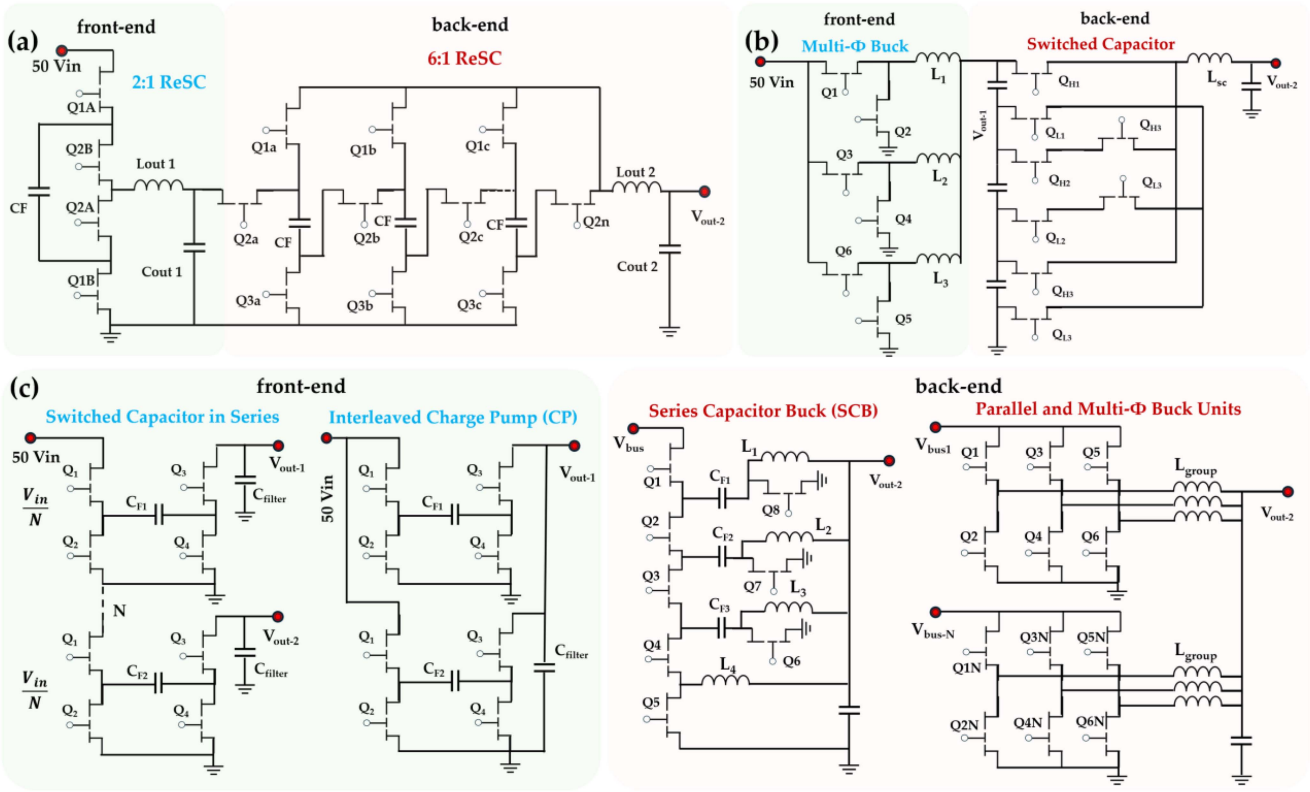


FIGURE 17. 50 V to PoL circuit topologies: (a) 2-stage resonant switched capacitor; (b) Dual bus with multi-Φ buck and switched capacitor; and (c) Front-end Switched capacitor/Interleaved charge pump and back-end series capacitor buck/multi-Φ buck converters.

CP front end followed by SCB modules (VIB), and an interleaved buck stage followed by an SC converter (dual-bus DC–DC converter). The two-stage ReSC converter cascades a 2:1 resonant SC front end with a 6:1 hybrid series–parallel resonant SC stage as shown in Fig. 17(a). Both stages transfer charge resonantly under ZVS operation, while all flying capacitors sustain only the output voltage, thereby eliminating charge-sharing and switching losses. Fig. 17(b) shows the circuit schematics of front-end SC/Interleaved CP and back-end SCB/multi-Φ buck. The SC + SCB converters combine a fixed-ratio SC front end with multiphase SCB modules through switching buses, eliminating bulky intermediate bus

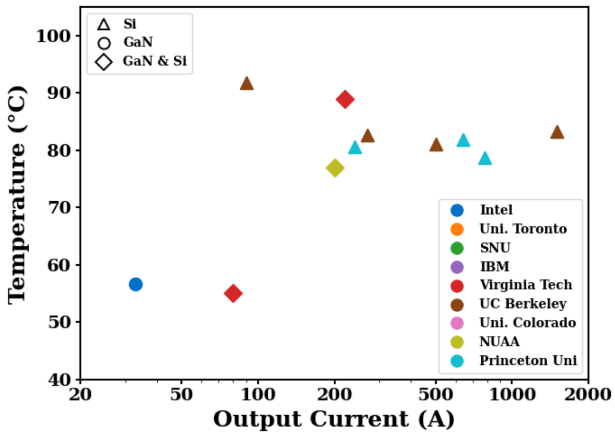


FIGURE 18. Operating temperature vs output power for 11 LV IBC 50 V-to-PoL V designs with reported thermal data.

capacitors. The Dickson[2] converter achieves most of the voltage step-down through a 9:1 SC stage, whereas the Hybrid-SC converters employ a simple 2:1 SC front end followed by deep 8:1/10-branch SCB modules to minimize switch voltage–current stress. In both cases, the SCB inductors soft-charge the flying capacitors, while interleaved PWM control regulates the output and balances phase currents. The VIB converter extends this concept, employing a 2:1 interleaved SC divider as its interleaved CP front-end, followed by four parallel four-level SCB modules. Using a ripple-tolerant 24-V virtual intermediate bus, the integrated stages eliminate first-stage inductors and bus capacitors, while the SCB inductors soft-charge the CP capacitors and interleaved PWM regulates the 1-V output. The SC + buck converters cascade an unregulated SC step-down stage with a multiphase interleaved buck regulator through minimal intermediate capacitance. Unlike SCB modules, where flying capacitors within the buck phases provide additional voltage division, the buck stage relies solely on duty-cycle regulation, simplifying the regulation stage. The LEGO converter employs series-stacked 2:1 SC cells to create stacked voltage domains that feed paralleled coupled-inductor buck phases, whereas the CaSP converter combines a 6:1 cascaded series–parallel SC ladder with a 3-Φ interleaved buck to achieve a higher SC conversion ratio and doubled inductor ripple frequency. In both topologies, the buck inductors soft-charge the flying capacitors, while the SC stage enables phase current sharing and the buck stage provides output regulation and fast transient response. The dual-bus converter reverses the stage order of SC + buck architectures by placing a four-phase interleaved buck stage at the 48-V input to regulate a 12-V intermediate bus, followed by a switched-capacitor voltage selector that further steps down the voltage to 4 V at high current as shown in Fig. 17(c). This arrangement places regulation on the lower-current side, relaxing duty-cycle and switch stress constraints, while the fixed-ratio SC output stage efficiently handles the high-current load.

Fig. 18 shows the relationship between output power and operating temperature. At moderate current levels, designs such as Sigma (80 A, 55°C) and CaSP (90 A, 91.8°C) operate comfortably within air-cooled limits. However, as output current scales into the hundreds of amperes, the 100°C operating-temperature boundary emerges as a practical thermal constraint. This trend is evident in LEGO and VIB, where liquid cooling increases current capability from 450 A to 780 A and from 350 A to 640 A, respectively, under similar thermal limits, demonstrating that cooling becomes the primary constraint on current scaling once the converter architecture is fixed. The Hybrid SC 1500 A similarly sustains 1300 A under air cooling before requiring enhanced thermal management for continuous operation above 85°C. The hybrid ReC represents a low-temperature outlier, recording 77°C at 200 A despite its relatively high power density, indicating a comparatively low loss density among the surveyed designs. Across the surveyed designs, increasing output current is accompanied by a progression from passive air cooling to forced-air and liquid-cooling solutions, highlighting the growing importance of thermal management as current demand increases.

Beyond thermal constraints, direct 50 V-to-PoL converters must satisfy stringent transient-response requirements because they replace the conventional VRM stage. However, only four surveyed designs report transient-response data, highlighting a significant reporting gap relative to efficiency and power-density metrics. Among the reported results, VIB exhibits the smallest voltage excursion, with an 80 mV peak-to-peak deviation for a 50–350 A load step at 4 A/µs. Mini-LEGO and LEGO-PoL report 100 mV and 120 mV excursions, respectively, with recovery times of 12–16 µs, demonstrating stable closed-loop operation despite their large conversion ratios and high output currents. Compared with the 12 V-to-PoL VRMs discussed previously, direct-conversion architectures exhibit less competitive transient performance. State-of-the-art VRMs, such as 180 A 6-Φ buck and 100 A IP-TLVR, achieve normalized voltage deviations of approximately 0.50–0.53 mV/A, substantially lower than those reported for direct 50 V-to-PoL converters. This is expected because VRMs are optimized solely for voltage regulation, whereas direct-conversion architectures must simultaneously perform high-ratio voltage conversion and regulation within a single power stage. Voltage excursions appear to depend more on controller design and output-energy storage than on topology, suggesting that future improvements will likely come from advanced control techniques.

D. TWO-STAGE VS SINGLE-STAGE CONVERSION FOR POL

The preceding analysis of LV IBCs, VRMs, and direct 50 V-to-PoL converters enables a comparison of the two principal AI server tray power-delivery architectures: the conventional two-stage approach, combining an LV IBC and VRM, and the emerging single-stage direct-conversion approach. From an efficiency perspective, two-stage performance is governed primarily by the VRM, since the LV IBC is typically highly efficient. By eliminating an entire conversion stage and the

associated intermediate bus losses, direct conversion can outperform many two-stage solutions. However, when paired with state-of-the-art GaN-based multiphase VRMs, two-stage architectures achieve comparable end-to-end efficiency, indicating that the efficiency advantage of direct conversion is most significant relative to mid-tier VRM implementations. In terms of power density and integration, direct conversion benefits from eliminating the intermediate bus and associated passive components, enabling the highest densities through board-level and ultimately on-package integration. This trend culminates in vertical power delivery (VPD), where the final conversion stage is mounted beneath the processor, replacing long lateral current paths with a short vertical path through the PCB [162], [164]. As processor currents approach the kilo-ampere regime, VPD reduces PDN resistance, I^2R losses, and impedance, improving both efficiency and transient response [163]. However, VPD imposes stringent constraints on converter height, current density, and thermal management, making low-profile magnetics and advanced cooling essential [86], [144]. Despite these advances, two-stage architectures retain greater placement flexibility by allowing the LV IBC to be located away from the processor while only the compact VRM occupies the socket region.

Regarding scalability and implementation maturity, two-stage architectures benefit from independent stage optimization, mature multiphase control, proven current sharing, and straightforward redundancy. In contrast, direct-conversion architecture introduces challenges such as flying-capacitor balancing, startup and protection sequencing, and tightly coupled regulation dynamics, although recent modular implementations have begun to address these limitations. Thermal and transient-response performance also favor the two-stage approach. Distributing losses between the IBC and VRM simplifies heat removal, whereas direct converters concentrate losses near the processor, making thermal management increasingly difficult as current scales. Similarly, dedicated VRMs provide faster and more tightly regulated transient response, while the intermediate bus capacitance buffers rapid load transients. Direct converters must simultaneously perform high-ratio conversion and regulation, resulting in larger voltage excursions and a less mature transient-response ecosystem. Overall, direct conversion offers advantages in integration and potential power density, whereas two-stage architectures remain superior in scalability, thermal management, transient response, and implementation maturity. Vertical power delivery is emerging as a complementary integration strategy that both architectures must ultimately adopt to sustain the current demands of next-generation AI processors.

V. SEMICONDUCTOR ANALYSIS FOR POWERING AI SERVERS

While the preceding sections examined power-conversion architectures and converter-level performance across the AI data center power delivery chain, the achievable efficiency, switching frequency, power density, and cost of each conversion stage are ultimately bounded by the underlying power semiconductor technology. This section therefore presents a comparative analysis of commercially available power devices, benchmarked from an extensive commercial database across key device-level metrics including the switching figure of merit (Ron × Qg), package area, current rating, and cost. The analysis is organized according to the two most demanding conversion stages identified earlier: for the HVDC isolated IBC interfacing the 800 V distribution bus, 1200 V SiC MOSFETs are evaluated against 650 V GaN HEMTs, where the trade-off between voltage robustness and switching performance governs topology and architecture selection; for the low-voltage IBC and VRM stages, low-voltage Si MOSFETs are benchmarked against emerging 15–100 V GaN HEMTs, where extreme current delivery, sub-1 V regulation, and socket-area constraints dominate device requirements. By mapping the commercial device landscape onto these application demands, the analysis identifies where WBG technologies have already surpassed incumbent silicon solutions and where adoption barriers in cost, packaging, and maturity remain.

A. 800 V HVDC SEMICONDUCTOR ANALYSIS

In the HVDC power path, the IBC that converts 800 V to 50 V represents one of the most challenging switching stages. The converter must maintain high efficiency, high power density, EMI, and reliable thermal performance within the confined space of modern server systems. As summarized in Table 6, 1200 V SiC MOSFETs and 600/650 V GaN HEMTs dominate primary-side implementations, while 150/120 V GaN HEMTs have also emerged in some designs as viable device technologies for this application. SiC devices are well suited for high-voltage and high-temperature operation owing to their high critical electric field and superior thermal conductivity [165], [166], whereas GaN devices benefit from high electron mobility and two-dimensional electron gas (2DEG) channel conduction, which enable extremely low on-resistance and reduced parasitic capacitances [51], [52]. These intrinsic material advantages directly impact switching loss, conduction performance, achievable switching frequency, and ultimately system-level power density [126], [167], motivating the comparative analysis presented in the following sections.

The Ron × Qg product is a key switching figure of merit because it captures the tradeoff between conduction and switching performance. Fig. 19(a) and (b) show the relationship between Ron × Qg and current rating for commercial 1200 V SiC MOSFETs and 650 V GaN HEMTs, respectively. A lower Ron × Qg indicates lower conduction and switching losses, enabling higher switching frequencies without a significant increase in gate-drive power or transition losses. Commercial 1200 V SiC MOSFETs exhibit Ron × Qg values ranging from approximately 1 to 10 nC·Ω over current ratings of 10–400 A. Devices below 50 A show considerable variation, with several products exceeding 4–8 nC·Ω, reflecting differences in die architecture and trench-gate process

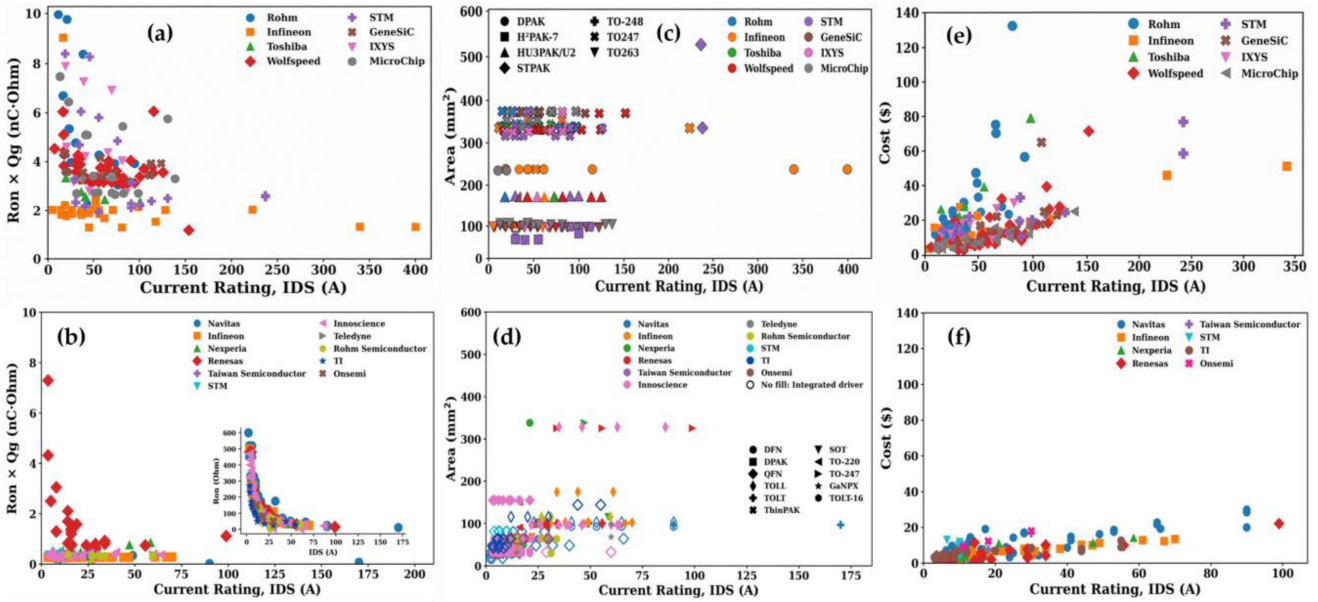


FIGURE 19. **Commercial 1200 V SiC MOSFET and 600–650 V GaN HEMT benchmarking for HVDC IBC applications: (a), (b) Ron × Qg vs. IDS; (c), (d) Area vs. IDS; and (e), (f) Cost vs. IDS.**

maturity [53]. Above 100 A, the devices converge toward 2–4 nC·Ω, while the best 300–400 A devices approach 1–2 nC·Ω through optimized trench-MOSFET structures that reduce Miller charge and switching losses. In contrast, commercial 650 V GaN HEMTs maintain Ron × Qg values below 1 nC·Ω across a wide current range of 25–175 A. Devices typically achieve 0.2–0.5 nC·Ω, representing a four- to tenfold improvement over similarly rated SiC devices. This advantage stems from very low Ron, and the lateral device structure, which eliminates body-diode reverse-recovery losses. The difference in Ron × Qg directly influences converter topology. Commercial 1200 V SiC MOSFETs can directly block the full 800 V bus, enabling conventional HB/FB topologies, whereas GaN-based HVDC IBCs typically employ ISOP architectures that distribute the bus voltage across multiple lower-voltage modules. Within this framework, GaN's lower Ron × Qg supports near-1 MHz operation, significantly reducing magnetic component size and increasing power density. Consequently, reported ISOP GaN LLC converters achieve power densities of 2100–2600 W/in^3, including 2514 W/in^3 (EPC), 2600 W/in^3 (STM), and 2100 W/in^3 (Navitas), substantially exceeding those of single-stage SiC converters, which remain constrained by lower switching frequencies.

The physical footprint of a power-device package has a direct impact on converter power density, parasitic inductance, thermal performance, and PCB layout efficiency, making package size a critical design factor in high-density AI server IBCs. Fig. 19(c) and (d) show the relationship between area and current rating for commercial 1200 V SiC MOSFETs and 650 V GaN HEMTs, respectively. Commercial SiC MOSFETs are predominantly packaged in through-hole form factors such as TO-247, TO-248, HU3PAK/U2, and STPAK, with typical footprint areas clustered around approximately 350 mm^2, 240 mm^2, 165 mm^2, and 100 mm^2, respectively. Each package family supports current ratings ranging from approximately 20 A to over 150 A. The high thermal conductivity of SiC (≈4.9 W/cm·K) enables larger die sizes and parallel die integration within a fixed package footprint, allowing current capability to scale without increasing package dimensions. Unlike SiC MOSFETs, GaN HEMTs are lateral devices with all terminals located on the top surface of the die, enabling advanced packaging techniques such as flip-chip, embedded-die, wafer-level chip-scale packaging, and copper-clip bonding [168]. Advanced packaging technologies such as GaNPX, ThinPAK, and TOLL enable compact footprints of only 10–100 mm^2 for GaN devices rated up to 100 A. In addition, integrated gate drivers reduce external driver circuitry and minimize parasitic gate-loop inductance, which is critical for suppressing gate ringing during GaN's ultra-fast switching transitions [169]. A key system-level consideration is that GaN-based IBCs typically require ISOP architectures, causing the effective semiconductor footprint to scale with the number of stacked modules. For example, a 60 mm^2 GaN switch position becomes approximately 120 mm^2 in a two-module ISOP design. Although ISOP architectures reduce GaN's apparent package-area advantage, GaN devices retain a significant density benefit through MHz-range switching, compact packaging, and integrated gate-driver solutions with minimal footprint overhead. Consequently, packaging technology remains a key enabler of the high power densities achieved by modern GaN-based HVDC IBCs.

Cost remains a key barrier to WBG adoption in hyperscale data centers, where small per-device price differences scale into millions of dollars across large deployments. Fig. 19(e) and (f) show the relationship between cost and current rating for commercial 1200 V SiC MOSFETs and 650 V GaN

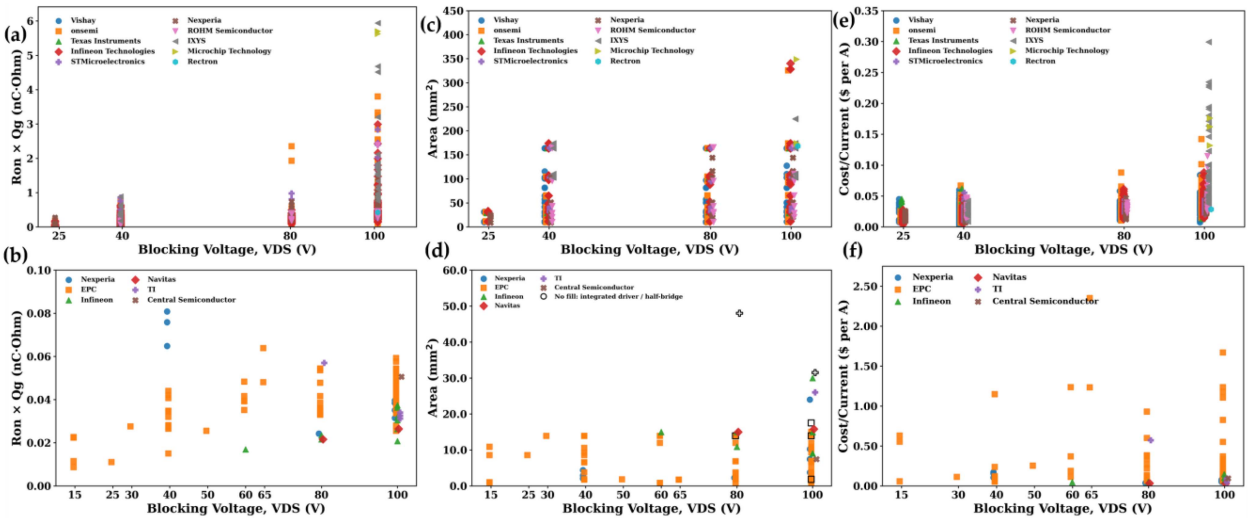


FIGURE 20. **Commercial LV Si MOSFET and GaN HEMT benchmarking for LVDC IBC applications: (a), (b) Ron × Qg vs. VDS; (c), (d) area vs. VDS; and (e), (f) Cost/current vs. VDS.**

HEMTs, respectively. For SiC MOSFETs, device prices range from approximately $5 to over $130 and generally increase with current rating. In contrast, GaN HEMTs exhibit a more favorable cost structure, with most devices priced between $2 and $25; many sub-50 A products cost less than $10, while even 75–100 A devices typically remain below $25. However, in an ISOP implementation, the effective device count increases; for example, an $8 GaN switch contributes approximately $16 at the converter level in a two-module stack. Although this reduces the apparent cost advantage of GaN, it does not eliminate it. The combination of lower Ron × Qg, compact packaging, and increasingly mature manufacturing processes continues to make ISOP-based GaN converters economically attractive for high-density 800 V HVDC IBCs in next-generation AI data centers. Overall, the combined benchmarking of Ron × Qg, package area, and cost indicates that GaN HEMTs are increasingly favored for high-density 800 V HVDC IBCs. Their superior switching performance, compact packaging, and competitive system-level cost enable MHz-range operation and highly integrated converter architectures. In contrast, SiC MOSFETs remain advantageous in applications that prioritize voltage blocking capability, thermal robustness, and high-current operation over switching frequency.

B. LVDC SEMICONDUCTOR ANALYSIS

The LV IBC and VRM stages discussed in Section IV represent the most demanding power-conversion challenge in modern AI servers, requiring thousands of amperes at sub-1 V with microsecond-scale transient response — constraints that place extreme requirements on the underlying semiconductor devices. Such requirements impose stringent constraints on switching and conduction losses, current density, package footprint, and cost. For decades, Si MOSFETs have been optimized to meet these demands. In contrast, LV GaN HEMTs have emerged as a key enabling technology owing to the intrinsic material and device-level advantages of the GaN structure. A growing body of work has demonstrated GaN-based LV IBC and VRM implementations employing LLC, resonant, hybrid switched-capacitor, and high-step-down converter topologies. The following analysis benchmarks commercial devices across five key metrics—Ron × Qg, package area, current rating, current density, and cost per ampere—to evaluate the transition toward GaN-based power conversion in AI-server LV power architectures.

Fig. 20(a) and (b) shows the Ron × Qg of commercial LV Si MOSFETs (25–100 V) and LV GaN HEMTs (15–100 V), highlighting the fundamental performance gap between the two device families. The Ron × Qg of LV Si MOSFETs increases sharply with blocking voltage, rising from approximately 0.1–0.3 nC·Ω at 25 V to 0.5–6 nC·Ω at 100 V. This voltage-dependent degradation originates from the inherent trade-off between blocking capability and conduction and switching performance in Si device structures, resulting from the thicker drift region and larger gate-drain charge required to sustain higher electric fields [75], [170]. In contrast, commercial GaN HEMTs compress this range to approximately 0.005–0.08 nC·Ω, providing nearly two orders of magnitude lower Ron × Qg than comparable Si MOSFETs. Values as low as 0.008 nC·Ω are achieved at 15 V, while even 100 V devices remain within the range of 0.02–0.065 nC·Ω. This superior Ron × Qg enables practical operation at MHz-range switching frequencies, as evidenced by the surveyed LV IBC and VRM implementations, where GaN devices are increasingly adopted to achieve high-frequency operation and higher power density.

Fig. 20(c) and (d) shows package-area benchmarking across the LV voltage range and reveals a fundamental divergence in footprint scaling between Si MOSFETs and GaN HEMTs. The package footprint of Si devices remains relatively constant at approximately 30–33 mm^2 across the 25–80 V range but increases nearly threefold to about 98

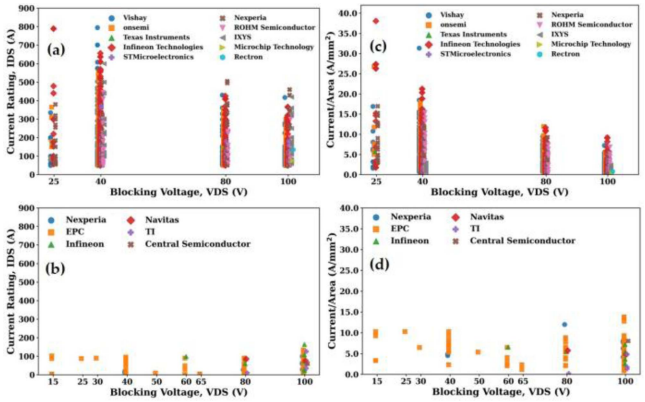


FIGURE 21. Commercial LV Si MOSFET and GaN HEMT benchmarking for LVDC IBC applications: (a), (b) IDS vs. VDS and (c), (d) IDS/area vs. VDS.

mm^2 at 100 V, driven by the transition to larger surface-mount and through-hole packages. This expansion reflects both the increased die area and thermal-management requirements associated with higher-voltage operation, ultimately limiting achievable converter power density. Si implementation is not limited to discrete MOSFETs. In VRM stages, monolithic BCD (Bipolar-CMOS-DMOS) power ICs integrate the power transistors, gate drivers, and control circuitry on a single die, reducing footprint and parasitic but remaining constrained in output-current capability by die area and thermal limits. In contrast, GaN HEMTs maintain a nearly constant footprint across the entire voltage range, with median package areas of approximately 8.6 mm^2 at 15 V and 7.5 mm^2 at 100 V. This flat scaling behavior is enabled by the lateral GaN device structure and the widespread adoption of LGA and wafer-level chip-scale packaging. The resulting footprint reduction enables higher passive-component integration density, greater thermal-layout flexibility around the processor socket, and power densities exceeding 1 kW/in^3 in AI-server LV power stages.

The current-rating and current-density landscape highlights the maturity gap between Si and GaN power devices. Fig. 21(a) and (b) shows the current rating and Fig. 21(c) and (d) shows current density of commercial LV Si MOSFETs and GaN HEMTs, respectively. Si MOSFETs offer a broad current range, spanning 50–800 A at 25 V, 50–650 A at 40 V, and 100–430 A at 80–100 V, while achieving current densities of 1–38 A/mm^2 across the 25–100 V range, with the best 25–40 V devices reaching 27–38 A/mm^2. GaN HEMTs currently operate within a narrower range, with most devices rated below 100 A and the highest-current offerings reaching approximately 100–170 A at 80–100 V. These limitations stem from the lateral GaN device structure, where current flows through a thin two-dimensional electron gas (2DEG) channel [171]. Scaling current therefore requires increasing gate width rather than bulk conduction area, introducing thermal stress, parasitic effects, and reliability concerns such as current collapse, inverse piezoelectric stress cracking, and electro migration [172], [173]. Consequently, commercial GaN HEMTs achieve current densities of approximately 0.5–14 A/mm^2 across the 15–100 V range. Wafer-level chip-scale devices at 15–40 V achieve 10–13 A/mm^2 through extremely compact packaging, while mainstream 100 V devices typically achieve 3–9 A/mm^2. As a result, despite its inferior switching FoM, Si continues to dominate high-current power stages owing to its superior current-handling capability and technological maturity, whereas GaN remains in the early stages of current-scaling development.

Fig. 20(e) and (f) shows that the cost-per-ampere metric reflects the maturity gap between established Si MOSFETs and emerging GaN HEMTs. LV Si MOSFETs across the 25–100 V range maintain a relatively narrow cost distribution of approximately \$0.01–0.10/A. In contrast, GaN HEMTs exhibit a much wider spread, with premium wafer-level chip-scale devices ranging from approximately \$0.05 to \$2.50/A owing to their specialized packaging and lower production volumes. However, commercial 80–100 V GaN products have converged toward \$0.01–0.15/A, approaching the cost-per-ampere levels of comparable Si MOSFETs. These trends suggest that while Si remains the benchmark for cost-effective current delivery, the commercial maturity of GaN is rapidly improving as device volumes increase and manufacturing costs decline. Overall, Si MOSFETs remain the dominant LV power device technology due to their high current capability, maturity, and cost advantage. GaN HEMTs, however, provide superior switching performance and footprint scaling, enabling higher-frequency and higher-density power conversion. Continued improvements in current capability and cost are expected to accelerate GaN adoption in future AI-server power architectures.

VI. CONCLUSION

The rapid growth of AI workloads is pushing rack power toward the megawatt level, exposing the scalability limitations of conventional AC-distributed architectures. Although modern 3–12 kW PSU's achieve efficiencies approaching 98%, further scaling is increasingly constrained by higher component count, cooling requirements, copper usage, rack-space consumption, and system complexity. Consequently, 800 V HVDC distribution has emerged as a promising next-generation solution, enabling reduced distribution losses, lower copper requirements, and improved rack utilization through centralized AC-to-DC conversion. The reviewed HVDC IBCs achieve efficiencies comparable to state-of-the-art PSUs while delivering power densities exceeding 2000–2600 W/in^3 through ISOP-based LLC architectures enabled by GaN devices.

At the server-tray level, the comparative analysis of LV IBCs, VRMs, and direct 50 V-to-PoL converters indicates that no single architecture simultaneously maximizes efficiency, power density, transient response, and thermal performance. For 50 V-to-12 V LV IBCs, resonant SC, LLC, and hybrid topologies achieve peak efficiencies above 98–99% and power densities exceeding 5000 W/in^3, with MHz-class GaN implementations defining the density frontier. In VRMs, topology

selection is closely linked to output current, with SC-based architectures favored below 10 A and multiphase buck, TLVR, and hybrid architectures dominating high-current applications due to their superior transient performance and scalability. Direct 50 V-to-PoL conversion eliminates the intermediate 12 V rail and associated losses, offering high integration and power density. However, the large conversion ratio imposes significant challenges in control, magnetics, thermal management, and transient response. Therefore, while direct conversion is expected to expand in highly integrated and package-level power delivery, the conventional two-stage LV IBC–VRM architecture remains the most practical and scalable solution for near-term high-power AI servers.

The device-level analysis highlights the critical role of WBG semiconductors in future AI power delivery. In HVDC applications, GaN HEMTs are increasingly becoming the preferred technology due to their ultra-low switching losses, negligible reverse recovery, and ability to enable high-frequency, high-power-density LLC and ISOP converter architectures. While SiC MOSFETs continue to offer advantages in voltage capability, thermal robustness, and high-power operation, the adoption trend is shifting toward GaN as converter architectures distribute voltage stress across multiple devices. At the board level, low-voltage GaN devices increasingly outperform silicon MOSFETs in switching performance, supporting MHz-class operation and reduced passive-component size. However, silicon MOSFETs continue to offer advantages in cost, maturity, and high-current applications, ensuring their continued relevance alongside WBG technologies.

Overall, the future AI power-delivery ecosystem is expected to evolve toward a hierarchical architecture consisting of centralized 800 V HVDC distribution, high-density ISOP-based HV IBCs, highly integrated LV conversion stages, and advanced package-level power delivery. Wide-bandgap semiconductors will be the key enabler of this transition, allowing simultaneous improvements in efficiency, power density, thermal performance, and scalability. As AI computing continues to push rack powers beyond the megawatt level and processor currents toward the kilo-ampere regime, the convergence of HVDC architectures, advanced converter topologies, and WBG semiconductor technologies will define the next generation of grid-to-chip power delivery systems for AI data centers.

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